International Journal of Advanced Information in Engineering Technology (IJAIET) ISSN: 2454-6933
Vol.5, No.1, January 2018

Recent Trends in Low Power VLSI Design

K.Deepa[1], M. Shirisha[2]
[1,2]Asst. Prof in ECE Department
[1,2]Samskruti College of Engineering &Technology.
Hyderabad

Abstract: The recent trends in the developments and advancements in the area of low power VLSI Design are surveyed in this paper. Though Low Power is a well-established domain, it has undergone lot of developments from transistor sizing, process shrinkage, voltage scaling, clock gating, etc., to adiabatic logic. This paper aims to elaborate on the recent trends in the low power design.

Key words: Multi threshold, dynamic voltage and frequency scaling, split level charge recovery logic, efficient charge recovery logic, positive feedback adiabatic logic, pre-resolve and sense adiabatic logic.

1. Introduction

1.1. Classification of Power Consumption

Though there are different types of power consumption, the major types that affect CMOS circuits are dynamic power and leakage power.

1.1.1. Dynamic power

Dynamic power is the power that is consumed by a device when it is actively switching from one state to another [3]. Dynamic power consists of switching power consumed while charging and discharging the loads on a device, and internal power (also referred to as short circuit power), consumed internal to the device while it is changing state [4]. Fig. 1 shows the dynamic power dissipation that can occur in CMOS circuits.

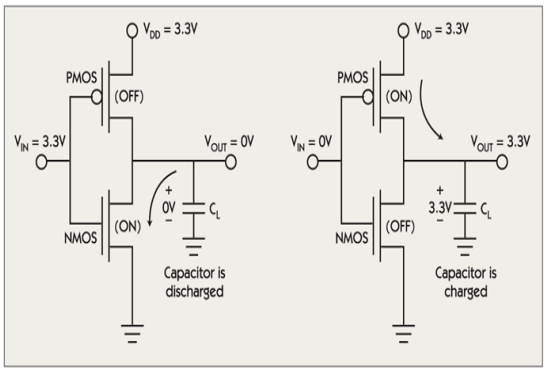


Fig. 1. Dynamic power reduction

1.1.2. Leakage power

Leakage power is the power consumed by a device not related to state changes [2]. Leakage power is actually consumed when a device is both static and switching, but generally the main concern with leakage power is when the device is in its inactive state, as all the power consumed in this state is considered "wasted" power .

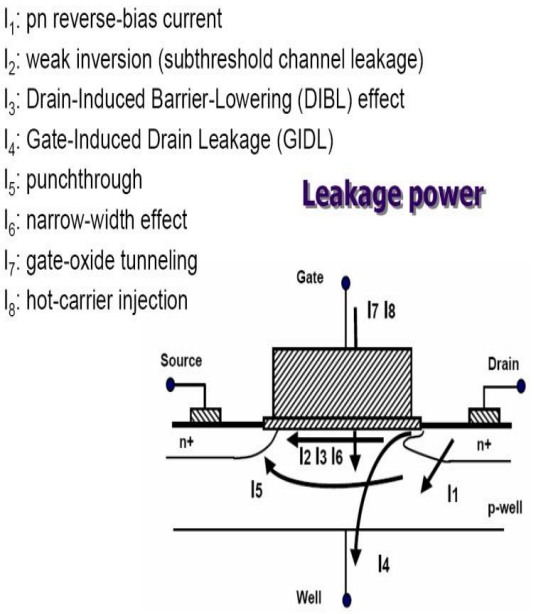


Fig. 2. Causes of leakage power

Different causes for the leakage power like reverse bias current, sub threshold channel leakage current, drain induced barrier lowering leakage, gate induced drain leakage, punch through, narrow width effect, gate oxide tunneling current, and hot carrier injection current are depicted in Fig. 2.Various techniques have been developed to reduce both dynamic and leakage power. CMOS circuit dynamic power consumption equation is

$$P=ACV^2FCLK$$

P is the power consumed, *A* is the activity factor, i.e., the fraction of the circuit that is switching, *C* is the switched capacitance, *V* is the supply voltage, and *F* is the clock frequency. If a capacitance of *C* is charged and discharged by a clock signal of frequency *F* and peak voltage *V*, then the charge

moved per cycle is *CV* and the charge moved per second is *CVF*. Since the charge packet is delivered at voltage *V*, the energy dissipated per cycle, or the power, is

Power=capacitive load* voltage^2*clock frequency

The data power for a clocked flip-flop, which can toggle at most once per cycle, will be half of the stated power. When capacitances are clock gated or when flip-flops do not toggle every cycle, their power consumption will be lower. Hence, a constant called the activity factor ($0 \leq A \leq 1$) is used to model the average switching activity in the circuit.

2. Traditional Power Reduction Techniques

To minimize this power, Technology scaling, voltage scaling, clock frequency scaling, reduction of switching activity, etc., were widely used.

The two most common traditional, mainstream techniques are:

Clock Gating:

Clock gating is a technique which is shown in Fig. 3 for power reduction, in which the clock is disconnected from a device it drives when the data going into the device is not changing. This technique is used to minimize dynamic power.

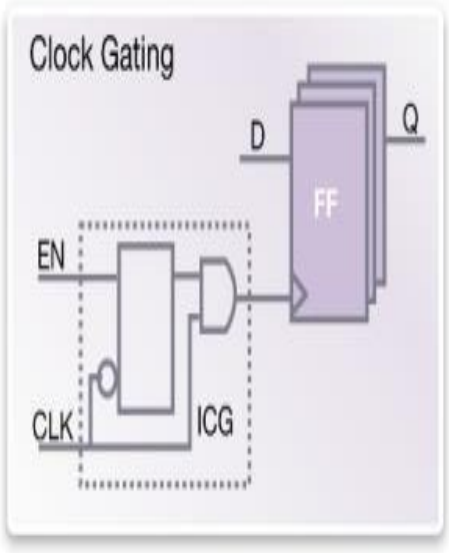


Fig. 3. Clock gating for power reduction.

Clock gating is a mainstream low power design technique targeted at reducing dynamic power by disabling the clocks to inactive flip-flops.

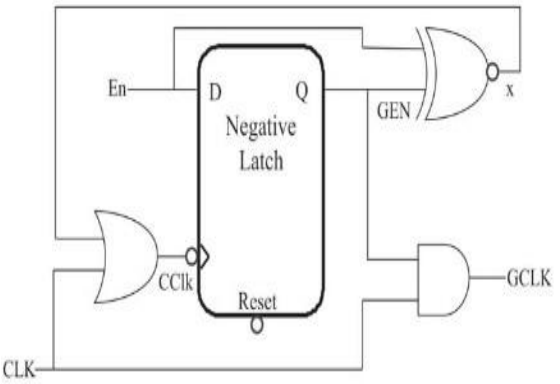


Fig. 4. Generation of gated clock when negative latch is used.

To save more power, positive or negative latch can also be used as shown in Fig. 4 and Fig. 5. This saves power in such a way that even when target device's clock is 'ON', controlling device's clock is 'OFF'. Also when the target device's clock is 'OFF', then also controlling device's clock is 'OFF'. In this more power can be saved by avoiding unnecessary switching at clock net.

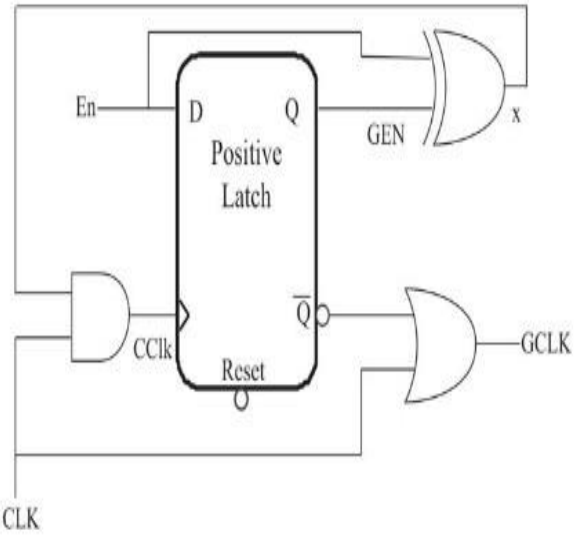


Fig. 5. Generation of gated clock when positive latch is used.

Multi-Vth optimization (Multi Threshold - MTCMOS):

MTCMOS is the replacement of faster Low-Vth (Low threshold voltage) cells, which consume more leakagePower, with slower High-Vth (high threshold voltage) cells, which consume less leakage power [7]. Since the High-Vth cells are slower, this swapping can only be done on timing paths that have positive slack and thus can be allowed to slow down. Hence multiple threshold voltage techniques use both Low Vt and High Vt cells. It uses lower threshold gates on critical path while higher threshold gates off the critical path.

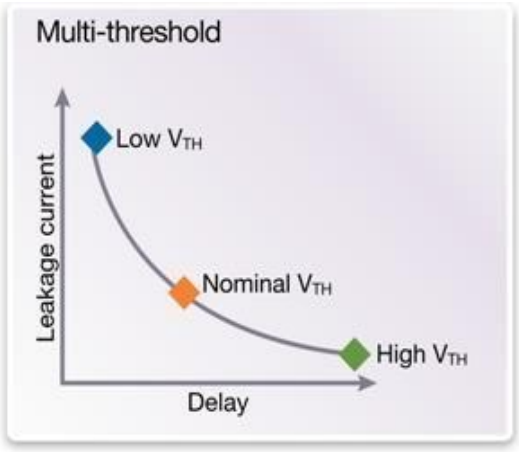
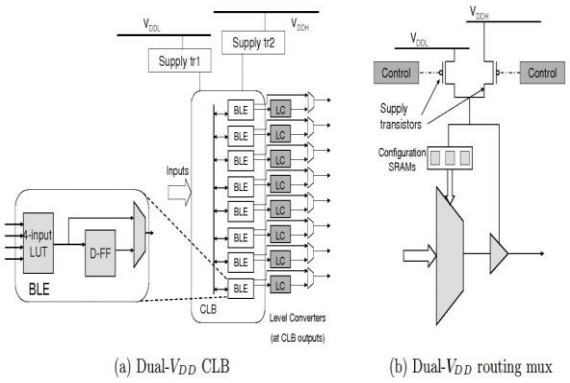


Fig. 6. Variation of threshold voltage with respect to the delay and leakage current

Fig. 6 shows the variation of threshold voltage with respect to the delay and leakage current. As Vt increases, delay increases along with a decrease in leakage current. As V_t decreases, delay decreases along with an increase in leakage current. Thus an optimum value of V_t should be selected according to the presence of the gates in the critical path. As technologies have shrunk, leakage power consumption has grown exponentially, thus requiring more aggressive power reduction techniques to be used. Several advanced low power techniques have been developed to address these needs. **The most commonly adopted techniques today are in below:**

1. Dual VDD

A Dual V_{DD} Configuration Logic Block and a Dual V_{DD} routing matrix is shown in Fig. 7.



(a) Dual-V_{DD} CLB (b) Dual-V_{DD} routing mux

Fig. 7. Dual V_{DD} architecture.

In Dual V_{DD} $architecture$ [10], the supply voltage of the logic and routing blocks are programmed to reduce the power consumption by assigning low-V_{DD} to non-critical paths in the design, while assigning high-V_{DD} to the timing critical paths in the design to meet timing constraints as shown in Fig. 8.However, whenever two different supply voltages co-exist, static current flows at the interface of the V_{DDL} Part and the V_{DDH} part. So level converters can be used to up convert a low V_{DD} to a high V_{DD}.

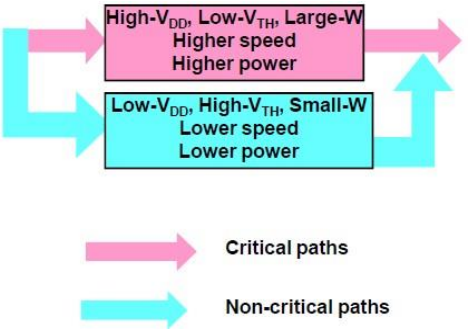


Fig. 8. High VDD for critical paths and low VDD for non-critical paths.

2) Clustered Voltage Scaling (CVS):

This is a technique to reduce power without changing circuit performance by making use of two supply voltages [11]. Gates of the critical path are run at the lower supply to reduce power, as shown in Fig. 9. To minimize the number of interfacing level converters needed, the circuits which operate at reduced voltages are clustered leading to clustered voltage scaling

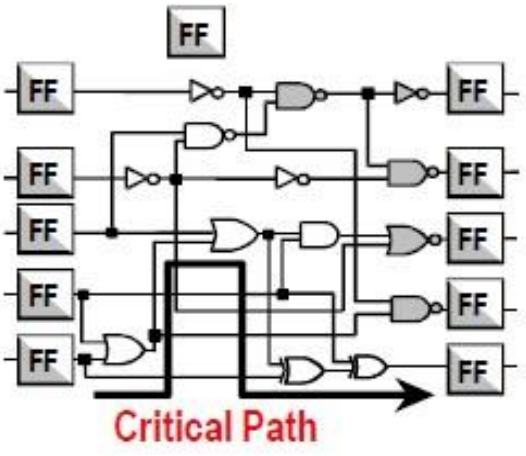


Fig. 9. Gates of the critical paths are run at lower supply.

Here only one voltage transition is allowed along a path and level conversion takes place only at flip-flops.

3) Multi-voltage (MV)

MV deals with the operation of different areas of a design at different voltage levels [9]. Only specific areas that require a higher voltage to meet performance targets are connected to the higher voltage supplies. Other portions of the

design operate at a lower voltage, allowing for significant power savings. Multi-voltage is generally a technique used to reduce dynamic power, but the lower voltage values also cause leakage power to be reduced.

4) Dynamic Voltage and Frequency Scaling (DVFS)

Modifying the operating voltage and/or frequency at which a device operates, while it is operational, such that the minimum voltage and/or frequency needed for proper operation of a particular mode is used is termed as DVFS, Dynamic Voltage and Frequency Scaling [12].

5) Adaptive Voltage Scaling (AVS)

Adaptive Voltage Scaling (AVS) provides the lowest operation voltage for a given processing frequency by utilizing a closed loop approach [13]. The AVS loop regulates processor performance by automatically adjusting the output voltage of the power supply to compensate for process and temperature variation in the processor [14]. In addition, the AVS loop trims out power supply tolerance. When compared to open loop voltage scaling solutions like Dynamic Voltage Scaling (DVS), AVS uses up to 45% less energy as shown in Fig. 10.

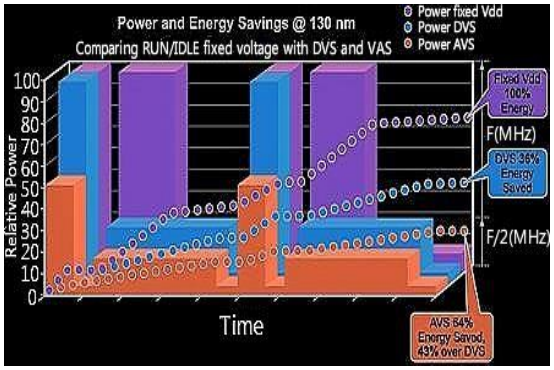


Fig. 10. Comparison of fixed voltage, DVS, and AVS energy savings in a processor

AVS is a system level scheme that has components in both the processor and power supply. The Advanced Power Controller (APC) provides the AVS loop control and resides on the processor. The Slave Power Controller (SPC) resides on the power supply and interprets commands from the APC. The IP provided in the APC and SPC automatically handle the handshaking involved in frequency and voltage scaling, simplifying system integration in the application.

3. Conclusion:

Thus Energy Recovery logic paves way for reusing the power in high speed power hungry circuits. This logic can be used in memories to save power to a greater extent.

References:

1) Weste, N., & Eshraghian, K. (1993). *Principle of CMOS VLSI Design: A System Perspective*, 2nd ed. New York: Addison–Wesley.
2) Roy, K., *et al*. (February 2003). Leakage current mechanisms and leakage reduction techniques in deep submicrometer CMOS circuits. *Proceedings of the IEEE, 91(2),* 305-327.
3) Kathuria, J., Ayoubkhan, M., & Noor, A. (Aug. 2011). A Review of clock gating techniques. *MIT International Journal of Electronics and Communication Engineering, 1(2),* 106-114.
4) Retrieved from the website: http://www.synopsys.com/advanced-low-power-techniques.aspx
5) Tawfik, S. A. (May 2009). Low power and high speed multi threshold voltage interface circuits. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 17(5).*
6) Dokić, B. L. (2013). A Review on energy efficient CMOS digital logic. *ETASR - Engineering, Technology & Applied Science Research, 3,* 552-561.