International Journal of Advanced Information in Engineering Technology (IJAIET) ISSN: 2454-6933
Vol.5, No.1, January 2018

New Technique for Reduction of THD in Single and Three Phase Multilevel Inverter

K.Sridhar[1], M.Bhasker[2]
[1, 2] Assistant Professor, [1, 2] Department of EEE,
[1,2] Samskruti College of Engineering & Technology, Hyderabad
[1]komatisridhar@gmail.com,[2]bhaskersagar7@gmail.com

Abstract: Many recent multilevel inverter papers end up with voltage Total Harmonic Distortion (THD) values obtained from numerical voltage spectrum calculations (measurements). Motivated by IEEE Standard 519, a part of multilevel research community uses a limited harmonics count to evaluate multilevel voltage quality. First, this causes significant voltage THD underestimation, especially, for relatively high frequency PWM. Second, for a three-phase star-connected balanced load with an isolated neutral and phase symmetric modulation strategy, calculated load line and phase voltage THD become different. However, simple considerations show that line and phase voltage THD are essentially the same in this case. It may be difficult to judge about multilevel voltage quality given a numerically calculated (measured) voltage THD value that may be subject to computation errors. Presented are simple smooth hyperbolic voltage THD upper and lower bounds approximations for single- and three-phase inverters with nearest synchronous switching. They are valid for arbitrary modulation indices and uniformly distributed levels counts and may practically serve as good reference values.

Index Terms–Multilevel inverters, DC-AC power conversion, Pulse width modulated power converters, voltage THD.

1. INTRODUCTION

Multilevel inverters are being widely used for medium / high voltage and other applications [1]-[5]. Many recent multilevelinverter papers end up with voltage THD evaluation resultsthat are typically based on voltage frequency spectra numerical calculations / measurements (FFT).A part of multilevel research Community uses a limited Harmonics count (49 Recommended by IEEE Standard 519 [6] or other like 101) to evaluate multilevel voltage quality. First, this causes voltage THD underestimation that is especially significant for relatively high frequency PWM (an error may reach 100% and more). Second, for a practical case of a three phase inverter with a star-connected balanced load with an isolated neutral, THD of line (line-to-line) voltage and that ofphase (line-to-neutral) one become different. However, simple time domain and symmetry based considerations show that line and phase voltage THDs are the same in this case. Some papers on cascade H-bridge three-phase converter with fundamental switching like [7] and [8] may Seem misleading as they talk about different line and phase voltage THDs.Indeed, for inverter side, phase (phase to inverter neutral) and line voltage THDs are different. However, for a star-connected balanced load with an isolated neutral, line andphase (phase to load neutral) voltage THDs have to be the same that is demonstrated below. Theoretical upper bound that is achieved for an infinitely high switching frequency is practically quite accurate for theratios of switching and fundamental frequencies that are largerthan 25-30 and is valid for both single and three-phase inverters [9]. Theoretical voltage quality lower bound is achieved for a minimum amount of synchronous switching thatis once between any two adjacent voltage levels [10], [11].Suggested are simple voltage THD upper and lower bounds smooth approximations for the optimal voltage quality nearestsynchronous switching for both single- and three-phase inverters. For cascaded H-bridge three-phase inverter, the relationship between inverter and load phase voltage quality is derived intime domain. It clearly demonstrates that the load voltageequality is better and its improvement comes at the expense ofload common-mode voltage deterioration. As the same equations are valid for the line and phase voltage fundamental components, they also hold for line andphase voltage ripples. The relationship

Between instantaneousline and phase voltage ripple squares from (1) becomes

$$v_{AB}^2 + v_{BC}^2 + v_{CA}^2 = 3(v_{AN}^2 + v_{BN}^2 + v_{CN}^2).$$

For a phase symmetrical modulation, after averaging on an AC fundamental period the three line voltage mean ripplesquares must be equal and so the three phase voltage ones.Then (2) means the equivalence between the line and phasevoltage THD because the ratio between the line and phasevoltage ripples RMS values representing undesired harmonics content and fundamental line and phase voltage harmonic magnitudes is the same $-\sqrt{3}$This way, the elementary time domain consideration accounting for the load and phase modulation symmetry [9] makes the above proof almost trivial while the same result in frequency domain is not so evident due to the fundamental difference between the line and phase voltage spectra.

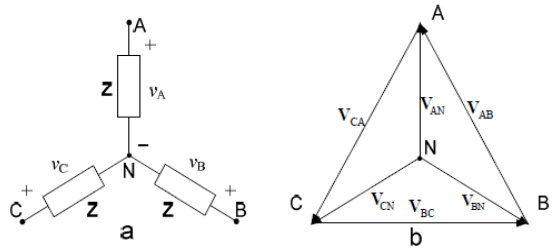

Fig. 1. Star-connected balanced three-phase load with isolated neutral: (a) schematic; (b) voltage-phasor diagram for a symmetrical load and supply.

III. VOLTAGE THD UPPER BOUND

Single- and three-phase multilevel inverters voltage quality for relatively high switching frequencies was considered in[10]. The results are valid for optimal voltage quality nearestlevel / virtual space vector switching and present theoreticalupper bound for synchronous switching. They are asymptoticin the sense that the ratio of the switching and fundamentalfrequencies is assumed infinitely large. Practically the formulasbecome quite accurate for the said ratio above 25-30. PWM voltage quality analysis is carried out in time domain using voltage ripple Normalized Mean Square (NMS) criterion(the voltages are normalized with respect to a DC bus one). Voltage ripple NMS is obtained by two successive averagingoperations - on a PWM period and on an AC fundamental one.The two averaging operations become independent due to the asymptotic assumption. Once the voltage ripple NMS is found,voltage THD can be calculated as

$$THD_n(m),\% = \frac{\sqrt{2NMS_n^{AC}(m)}}{m} \cdot 100[\%], \qquad (3)$$

n - (Non-negative) converter voltage level count (2 for a 2-level inverter);m - Modulation index, 0<m<1;$NMS_n^{AC}(m)$ - voltage ripple NMS expression.

For an arbitrary voltage level count, the voltage ripple NMS expression is piece-wise analytical, employs only elementaryfunctions and is given by formula (10) in [9]. Due to theasymptotic assumption (very high switching frequency), thevoltage ripple NMS formula does not contain frequency dependences. Initially obtained for a single-phase (H-bridge)multilevel inverter, formula (10) in [9] is valid for a three-phase inverter line voltage as well because the NMS criterionis invariant to voltage pulses re-distribution within a PWM period (zero sequence insertion).Some voltage THD graphs according to (3) are given in Fig.2, a. Voltage THD vs. *m* referred to *n*+1 levels is obtainedfrom that for *n* levels by scaling x-axis *S=(n-1)/n* times and adding the rightmost missing link for the *m* interval *(n-1) /n ≤m <1.*

Ignoring the NMS pulsation by using its average value [10]

$$NMS_{n\_AV}^{AC} = \frac{1}{6(n-1)^2}, \qquad (4)$$

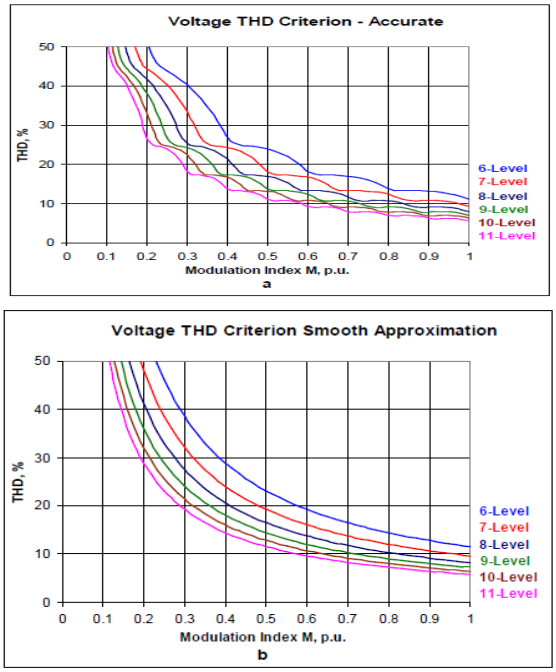

Fig. 2. Voltage THD upper bound for 6, 7, 8, 9, 10, 11 levels: a – accurate according to (3), (6); b – smooth approximation according to (5).

Voltage THD upper bound may be approximated in a ripple free smooth manner as [10]

$$THD_{SM}^{UP}(m,n),\% = \frac{1}{\sqrt{3}(n-1)m}\cdot 100\% = \frac{57.7}{(n-1)m},\%.$$

Formula (5) presents an approximate upper bound for both single- and three-phase inverters (Fig.2, b) with the worst case accuracy being better than 5% for sufficiently large modulation indices.

IV.VOLTAGE THD LOWER BOUND

Voltage quality lower bound is achieved for a minimal amount of nearest switching [10], [11] meaning switching oncebetween any two adjacent voltage levels that is staircase, orstep, modulation (Fig.3). Finding accurate voltage THD lower bound, in fact, means finding optimal switching angles that minimize quadratic approximation error (NMS). There are 2 major components of the associated optimization problem – problem formulation and solution method. The problem formulation in frequency domain as a global optimization problem accounting for a limited harmonic count is a potential source of inaccuracy. In combination with metaheuristic optimization, it delivers sensitive unstable solutions that don't provide reliable predictable optimal switching angles and voltage THD [12].

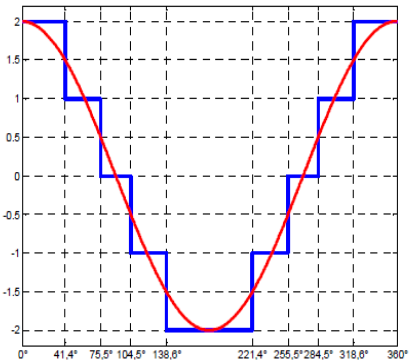

Fig. 3. Nearest switching strategy for a 3-level single-phase inverter.

This way, the optimization problem must be formulated in time domain as a constrained optimization one thus taking into account all switching harmonics. The constraint is due to a fundamental voltage (modulation index) requirement. The accurate expression for a quadratic error to be minimized may be easily obtained by the squared voltage approximation error (Fig.3) analytical closed-form integration. A similar approach was applied to find voltage THD lower bound local minima for different converter level counts (L=2…8) in [13], [14] and the results obtained in both papers are identical. Using IEEE Standard 519 recommended 49 harmonics count causes voltage THD underestimation that is about 7% for a 3-level inverter and progressively increases with the level count increase (e.g., about 16% for a 6-level converter) [15].Voltage THD lower bound is mostly of theoretical interest because as the minimum is "flat" it is a kind of ill-conditioned optimization problem and many different switching angles combinations can deliver near-optimal voltage quality. Similar to (4), (5), using optimal NMS average value that is numerically obtained NMS constant component for 0<m<1, voltage THD lower bound for single-phase inverters may be approximated in a smooth ripple-free manner as [10], [11]

$$THD_{SM}^{1.LOW}(m,n),\% = \frac{42}{(n-1)m},\%. \qquad (6)$$

Formula (6) ignores, as (5), THD pulsation and accurately renders the average trend with the worst case voltage THD error being of the order of 10% (of THD) for sufficiently large modulation indices. Maxima and minima of voltage THD lower bound may be addressed on separate if required.Most of the above considerations for a single-phase inverter voltage THD lower bound are applicable to a three-phase inverter one. However, for a three-phase inverter, the voltage THD lower bound is larger due to inter-phase dependences because the switching angles can't be selected independently and must fulfil additional constraints that arise from the quarter-wave symmetry and nearest switching requirements. Using symmetry considerations, by time averaging it can be shown that for a three-phase cascade H-bridge inverter with a balanced three-phase load with an isolated neutral

$$NMS_{Ph} = NMS_{PN} - NMS_{nN}, \qquad (7)$$

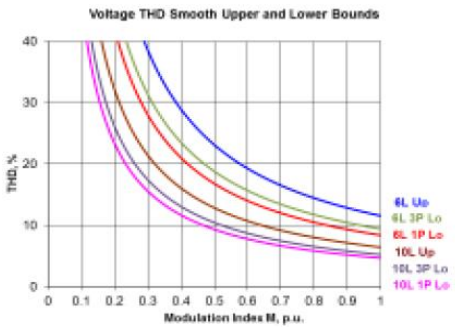

Fig. 4. Voltage THD smooths upper and lower bounds comparison for single and three-phase inverters for 6 and 10 levels.

Where ripple voltage NMS terms refer to load Phase-to-neutral, inverter Phase-to-Neutral and load neutral to inverter Neutral (common-mode) voltages. The major learning's from (7) are:

– load phase voltage THD (ripple voltage NMS) is less than inverter phase voltage one;

– Optimal load voltage quality – minimal load phase voltage THD (ripple voltage NMS) – is achieved at the expense of common-mode voltage THD (NMS) increase.For a three-phase inverter, voltage THD lower bound smooth approximation becomes [11]

$$THD_{SM}^{3,LOW}(m,n),\% = \frac{47}{(n-1)m},\% \qquad (8)$$

That is 12% larger than that for a single-phase one (6).

A 3-phase cascade H-bridge inverter load voltage THD bounds may be estimated based on line voltage waveform that has a non-negative level count equal to n= 2N (N – a number of cascaded 2-level H-bridges in a single phase). Voltage THD upper (5) and lower bounds (6), (8) smooth approximations comparison for 6 and 10 converter levels is presented in Fig.4.

V. CONCLUSION

It is shown that for a three-phase star-connected balanced load with isolated neutral and phase symmetrical modulation, line and phase voltage THD are basically the same independent on a multilevel inverter type employed. As the major multilevel voltage quality improvement comes from increased levels count, Selected Harmonics Elimination and similar techniques don't make much practical sense for a relatively high level count as long as there are no specific voltage spectrum requirements. Suggested simple hyperbolic voltage THD upper and lower bound approximations for single- and three-phase inverters are valid for arbitrary modulation indices and equidistant levels counts with a practical accuracy of 5-10% of voltage THD and may serve as reliable initial reference values for practical measurements and calculations often making numerical voltage THD calculations unnecessary.

REFERENCES

1) J. Rodriguez, S. Bernet, B. Wu, J.O. Pont, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," IEEE Trans. Ind. Electron., vol. 54, no. 6, pp. 2930-2945, Dec. 2007.
2) G. Buticchi, D. Barater, E. Lorenzani, C. Concari, and G. Franceschini, "A nine-level grid-connected converter topology for single-phase transformerless PV systems," IEEE Trans. Ind. Electron., vol. 61, no. 8, pp. 3951-3960, Aug. 2014.
3) L. Tariscioti, P. Zancheta, A. Watson, S. Bifareti, and J.C. Clare, "Modulated model predictive control for a seven-level cascaded H-bridge back-to-back converter," IEEE Trans. Ind. Electron., vol. 61, no. 8, pp. 3951-3960, Aug. 2014.
4) Buccella, C. Cecati, M.G. Cimoroni, and K. Razi, "Analytical method for patern generation in five-level cascaded H-bridge inverter using selective harmonic elimination," IEEE Trans. Ind. Electron., vol. 61, no. 11, pp. 5811-5819, Nov. 2014.
5) Mora, P. Lezana, and J. Juliet, "Control scheme for an induction motor fed by a cascade multicell converter under internal fault," IEEE Trans. Ind. Electron., vol. 61, no. 11, pp. 5948-5955, Nov. 2014.
6) IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems, IEEE Std. 519-1992, 1993.
7) N. Farokhnia, H. Vadizadeh, S. H. Fathi, and F. Anvariasl, "Calculating the formula of line voltage THD in multilevel inverter with unequal DC sources," IEEE Trans. Ind. Electron., vol. 58, no. 8, pp. 3359–3372, Aug. 2011.
8) N. Yousefpoor, S.H. Fathi, N. Farokhnia, H.A. Abyaneh, "THD minimization applied directly on the line-to-line voltage of multilevel inverters", IEEE Trans. Ind. Electron., vol. 59, no. 1, pp. 373–380, Jan. 2012.
9) Ruderman, B. Reznikov, S. Busquets-Monge, "Asymptotic time domain evaluation of a multilevel multiphase PWM converter voltage quality", IEEE Trans. Ind. Electron., vol. 60, no. 5, pp. 1999–2009, May 2013.
10) Ruderman, G. Mehlmann, and B. Reznikov, "PWM voltage quality bounds of a single-phase multilevel inverter," Proc. Int. Conf. on Optim. of Electr. and Electron. Equip. (OPTIM), May 2012, pp. 58-68.
11) G. Mehlmann, A. Ruderman and G. Herold, "Voltage quality bounds of multilevel inverters," Proc. Int. Energy Conf. & Exhib. (ENERGYCON), Sep 2012, pp. 90-97..
12) V. Roberge, M. Tarbouchi and F. Okou, "Strategies to accelerate harmonic minimization in multilevel inverters using a parallel genetic algorithm on graphical processing unit", IEEE Trans. Power Electron., vol. 29, no. 10, pp. 5087–5090, Oct. 2013.
13) C.A.L. Espinosa, I. Portocarrero, and M. Izquierdo, "Minimization of THD and Angles Calculation for Multilevel Inverters", Int. Journal of Eng87. & Technology IJET-IJENS, Oct. 2012, vol. 12, No. 05, pp. 83-86.
14) Fang Lin Luo, "Investigating of best switching angles to obtain lowest THD for multilevel DC/AC inverters", 8th IEEE Conference on Ind. Electron. and Applications (ICIEA '13), June 2013, pp. 1814-1818.
15) Diong, "THD-optimal staircase modulation of single-phase multilevel inverters", Trans. IEEE Region 5 Conference, Apr. 2006, vol. 12, pp. 275-279.

Author's Profile:

K.Sridhar, presently working as Assistant professor in Samskruthi College of Engineering and technology, Ghatkesar, Rangareddy, Telangana, India.completed the B. Tech degree in Electrical & Electronics Engineering from KTME, JNTU, Hyderabad. And then completed his M.Tech in Electrical & Electronics Engineering with PE specialization at STCET, JNTU, and Hyderabad. He has a teaching experience of 11

years. His areas of interest are Power System, Power Electronics and Electrical Drives, FACTS, Switchgear and Protection.

M.Bhasker presently working as Assistant professor in Samskruthi College of Engineering and technology, Ghatkesar, Rangareddy, Telangana, India.Completed the B. Tech degree in Electrical & Electronics Engineering from SICET, JNTU, and Hyderabad. And then completed his M.Tech in Electrical & Electronics Engineering with EPS specialization at JBIET, JNTU, and Hyderabad. he has a teaching experience of 1 years.His areas of interest are Power System, Power Electronics, FACTS, Switchgear and Protection.