LOW POWER BASED ECG DETECTOR FOR CARDIAC PACEMAKER

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Abstract- To achieve the low power design of wavelet based electrocardiogram (ECG) for implantable cardiac pacemaker is presented. The proposed wavelet based ECG detector consists of wavelet decomposer, QRS complex detector and noise detector with zero crossing points. To achieve the significant power consumption and QRS detection accuracy multi scaled product algorithm and soft threshold algorithm have been used in QRS complex detector. The standard0.9 µm CMOS technology has been used.

Index terms- Electrocardiogram, QRS complex detector, multi scaled product algorithm, soft threshold algorithm.

I.INTRODUCTION

Now a days reduced power consumption of bio medical devices taking an important role in health care industry. There are many implanted medical devices are available in medical industry such as electrocardiogram (ECG),electromyography (EMG), electroretiuogram (ERG) and electrooculography (EOG). These devices can be used to the patient and send current to various parts of a patient body. The implanted device has mainly two parts: there are internal part and an external part. The internal part located underneath the body skin and an external part. *i.e.*, controller. The external part mainly used for sending the date to outside world. Implantable devices are self-operating devices which adjust their operation depending upon the patient's condition. These devices do not rely on external sources of power. Thus, low power consumption and high data rate are the main requirements for medical implant devices. In order to minimize cost, patient trauma and risk associated with the repeated surgeries, it is necessary to increase the lifetime of implanted batteries by conserving energy at every stage of a device's operation.

The energy-efficient wavelet ECG detector for implantable cardiac pacemaker is proposed in this paper. The ECG detector consists of a wavelet decomposer with wavelet filter banks, QRS complex detector and noise detector with zero crossing points. In QRS complex detector there are two algorithms are exhibited. The multi-scaled product algorithm, which leads to the low power consumption. To boost the QRS detection accuracy the soft-threshold algorithm is used, which is implemented without large power and area.

The Electrocardiogram (ECG) detector checks the heart-beating rate and rhythm with the digitized ECG signals from an analog-to-digital converter (ADC). When an abnormal heart-beating is detected, electrical stimulations are applied to the heart using the high-voltage multiplier and pulse generator. In order to achieve a high guarantee of safety for the patients, high detection reliability is the most essential property of the cardiac pacemaker. Moreover,once it is implanted inside human body, the pacemaker is expected to operate over several years without changing the battery. To avoid repeated surgeries due to battery exhaustion, low power consumption is another extremely important design requirement for IPIC. According to previous research work, while the analog circuits including amplifiers and bias circuit take about half of the overall power consumption, the digital logic circuit including the ECG detector is the second power hungry block, which utilizes 15% or more.

II.METHODOLOGY

ECG detector

This project aims to achieve the high detection accuracy with low power consumption for wavelet based ECG detector for implantable cardiac pacemakers.

- To achieve the low power consumption multi-scaled product algorithm and soft threshold algorithm is used

Input from ADC

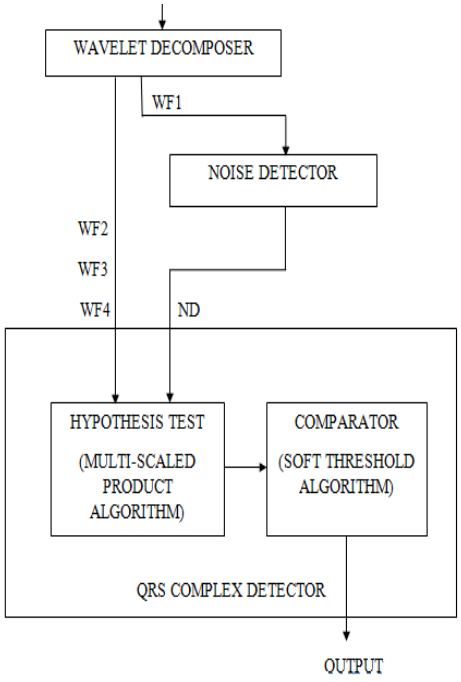

Fig 2.1 block diagram for ECG detector

2.1 Wavelet decomposer

The proposed ECG detector uses the wavelet decomposer. The decimation is the process of reduces the sampling rate of a signal. The decimator based wavelet decomposer implemented with the wavelet filter banks. The wavelet filter consists of low pass filter and high pass filter.

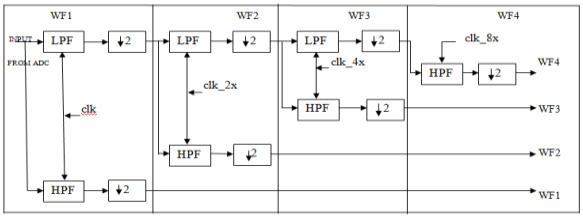

Fig 2.2 schematic diagram of wavelet decomposer

A low-pass filter is a filter that passes signals with a frequency lower than a certain cutoff frequency and attenuates signals with frequencies higher than the cutoff frequency. The amount of attenuation for each frequency depends on the filter design. A high-pass filter (HPF) is a filter that passes high-frequency signals but attenuates (reduces the amplitude of) signals with frequencies lower than the cutoff frequency.

2.2 Noise detector

The noise detector which consists of counter of zero crossing points , XOR gate and reset counter.

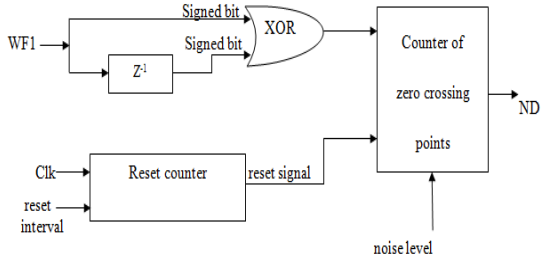

Fig 2.3 schematic diagram for noise detector

The noise level inside the ECG detector is measured by counting the number of zero crossing points in a certain time interval. The wf1 output passes to the xor gate and the previous value to be stored at register, the xor gate compares the current output and previous value. The output of xor gate passes to the counter, and it counts the signal for every zero crossing points. The reset counter used to reset the counter value for each clock pulse.

2.3 QRS complex detector

The QRS complex is an important part of the ECG signal which must be detected and we hope to be able to detect a peak signal of the ECG signal as well. This is why the design of the suitable detector circuit is required. The power consumption and the simplicity of the circuit is considered, because of the limitation in the area and power of a portable battery. Besides the circuit must be able to give a binary output for the detector. The proposed method

QRS complex detector uses the multi scaled product algorithm and soft threshold algorithm.

2.3.1 Multi scaled product algorithm

Hypothesis testing is an inferential procedure that uses sample data to evaluate which should be selected as an output. The purpose of hypothesis testing is to make a decision in the face of uncertainty.

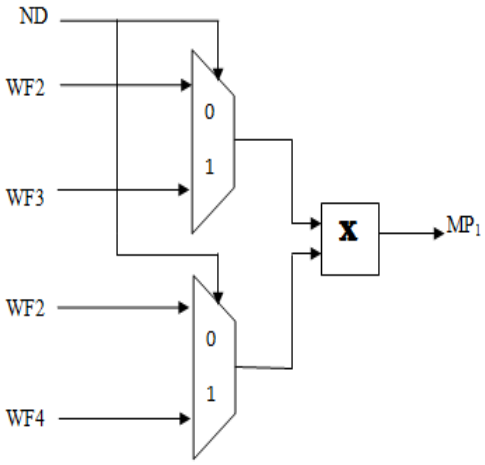

Fig 2.4 Multi scaled product algorithm

2.3.2 Soft threshold algorithm

Soft thresholding is a simple technique for denoising signals and images. When the signal is represented in terms of a wavelet basis,small coefficients are set to zero and larger coefficients above some threshold are possibly shrinked. Therefore, thresholding usually produces signals that are scattered and it will have only a small number of non-zero coefficient.

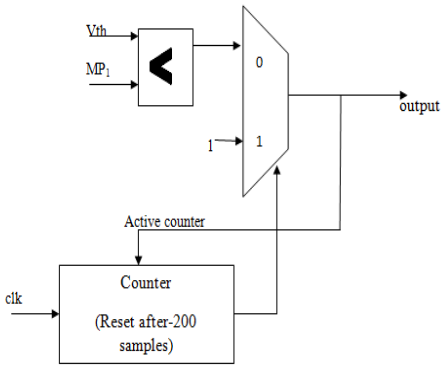

Fig 2.5 soft threshold algorithm

2.4 ADC implementation

Analog-to-digital converters (ADC) targeted for use in medical implant devices serve an important role as the interface between analog signal and digital processing system. Usually, low power consumption is required for a long battery lifetime. In such application which requires low power consumption and moderate speed, one of the most prevalently used ADC architectures is the successive approximation register (SAR) ADC.

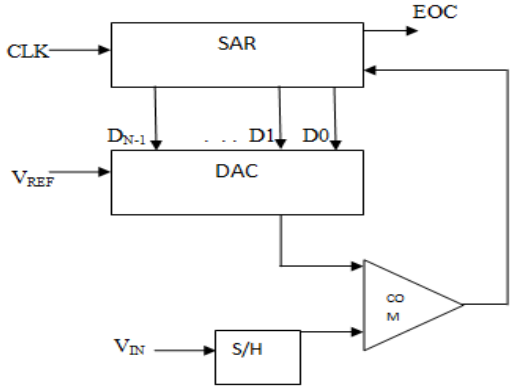

Fig 2.5 : Block diagram of SAR ADC

Successive approximation register (SAR) ADC is designed and it consists of a successive approximation register (SAR), a digital-to-analog converter, a comparator and a sample and hold circuit.

First, input voltage (V_{IN}) is sampled and the registers are reset to zero. Secondly, the conversion starts through an approximation of MSB (set MSB as one) by

SAR; DAC converts the digital information to a voltage V_{OUT} (half of the reference voltage V_{REF}); Comparator compares V_{OUT} with V_{IN}. If V_{IN} is larger than V_{OUT}, it outputs one, otherwise, it outputs zero; SAR loads the comparator result, registers the value of MSB and generates its next approximation; the conversion continues until the LSB is decided. Therefore, an N-bit SAR ADC needs N clock cycles per conversion.

III.TOOLS USED

The Architecture of the ECG detector is coded in VHDL. The entire Architecture is splited into wavelet decomposer, noise detector and QRS complex detector as component, each sub components are then coded separately and are instantiated in the main module. Then the code is compiled and synthesized using Xilinx ISE 8.1i and is simulated using the modeIsim 5.5E software. Then the power, Area and timing is compiled in design compiler using Synopsys tool.

IV. RESULTS AND DISCUSSION

4.1 Result of wavelet decomposer using decimator based wavelet filter bank

The output of the each wavelet filter bank of HPF is fed to the input of hypothesis test and the wf1 output is given to noise detector to choose the mode of selection.

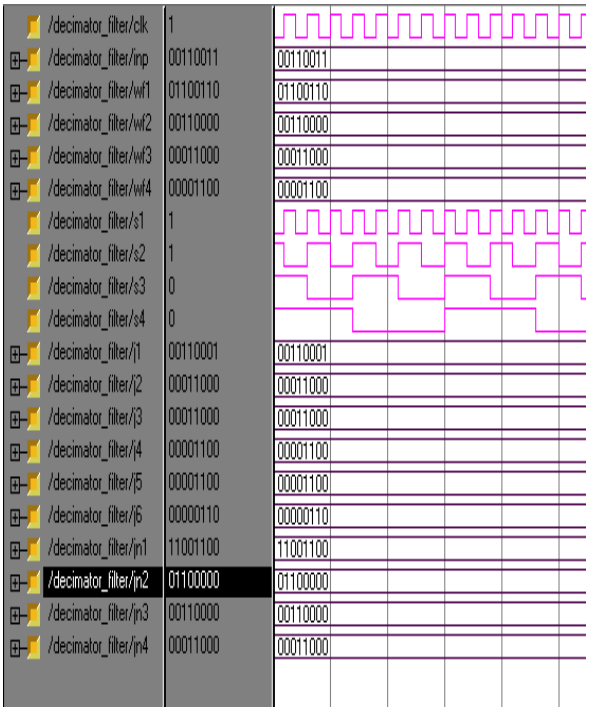

Fig 4.1 simulation result of decimator based wavelet decomposer

4.2 Result of noise detector

The wf1 output passes to the xor gate and the previous value to be stored at register, the xor gate compares the current output and previous value. The output of xor gate passes to the counter, and it counts the signal for every zero crossing points. The reset counter used to reset the counter value for each clock pulse.

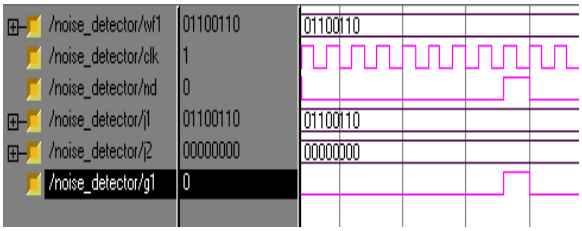

Fig 4.2: simulation result of noise detector

4.3 Result of QRS complex detector

4.3.1 Result of multi scaled product algorithm

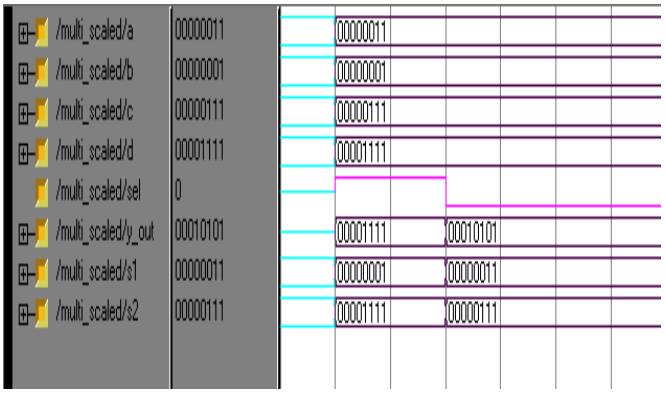

Fig 4.3: simulation result of multi scaled product algorithm

4.3.2 Result of soft threshold algorithm

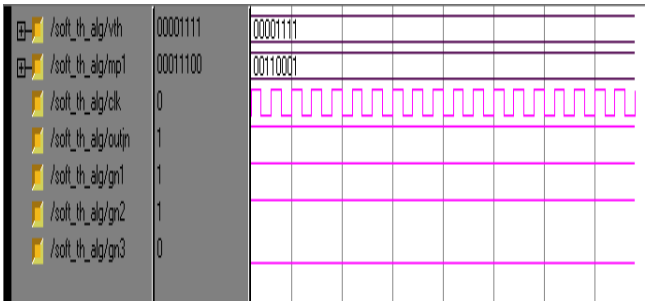

Fig 4.4: simulation result of soft threshold algorithm

QRS complex detector

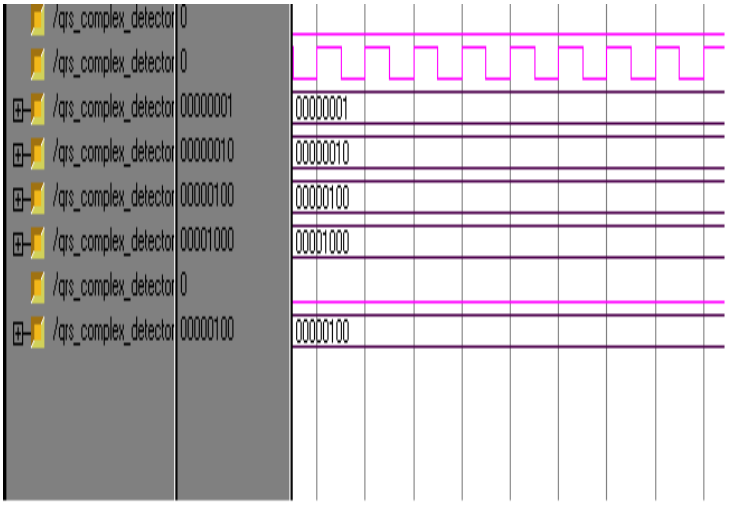

Fig 4.5: simulation result of QRS complex detector

4.4 Result of proposed ECG detector

Fig 4.6: simulation result of proposed ECG detector

4.5 Result of SAR-ADC

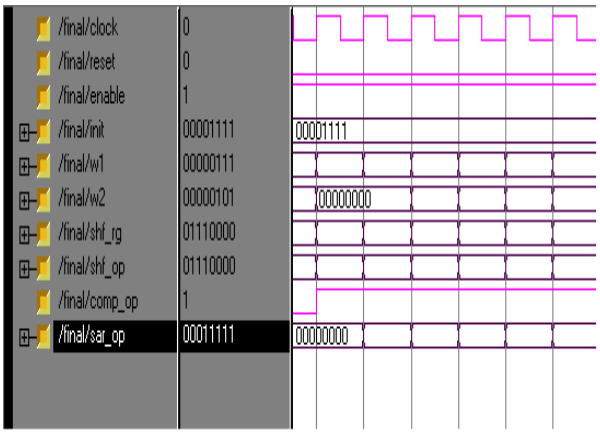

Fig 4.7: Simulation result of SAR-ADC

4.6 Synthesis result for proposed ECG detector

Component	Utilization
Multipliers	1
8 x 8 bit multiplier	1
Adders/ subtractors	17
10-bit adder	16
12-bit adders	1
Counters	3
32-bit up counter	1
8-bit up counter	2
Registers	6
1-bit register	5
8-bit registers	1
Latches	16
1-bit latches	3
9-bit latches	13
Comparators	3
8-bit comparator greater	2
8-bit comparator lessequal	1
XOR gate	1

4.7 Synopsys tool

Synopsys is one of the ASIC implementation. The Application-Specific Integrated Circuit (ASIC) is an integrated circuit (IC) customized for a particular use, rather than intended for general-purpose use. ASIC are used for low power and high speed design. Here the power and area for ECG detector is analyzed by using 90 nm technology.

4.7.1 Area report

Parameter	Area
Combinational area	21124.391987
Non combinational area	3422.263004
Net Interconnect area	318.231654
Total cell area	24546.654992
Total area	24864.886645

4.7.2 Power report

Parameter	Power(µW)
Global Operating Voltage	1.32
Cell Internal Power	130.5403
Net Switching Power	204.8024
Total Dynamic Power	335.3427
Cell Leakage Power	283.7405
Total Power Group	0.6191

V CONCLUSION

A low power ECG detector for implantable cardiac pacemaker is proposed in this paper. In order to achieve the low power consumption multi scaled product algorithm and soft threshold algorithm is proposed. Proposed ECG detector implemented with successive approximation analog to digital converter (SAR-ADC) using 0.9µm CMOS technology. The proposed ECG detector requires less power. Moreover, the application can be extended to overall battery operated biomedical healthcare devices.

VI REFERENCES

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