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Introduction Of Partial Power Conversion Device Without Large Electrolytic Capacitors And Comparison Of Various Power Flow Control Methods

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***Abstract*— A partial power conversion device (PPCD) is proposed to realize power flow control and voltage compensation in a three-phase power distribution system in this paper. The PPCD circuit, which is derived from the conventional push–pull forward converter, can achieve arbitrary voltage output without any large electrolytic capacitors. Thus, the system reliability can be enhanced. Furthermore, the converter has no full-rated components,which reduces the cost. In this paper, comparison of various power flow control metods such as traditional offline methods and new FACT device are done and also an injection model for power flow control is derived.A closed-loop control method employing the synchronous reference frame theory for voltage compensation is also developed to enable the precise control. The systems with PPCD are simulated byMATLAB/Simulink to verify the functions. The experiments for voltage compensation are carried out based on a 30-kW prototype,which shows the effectiveness.**

Keywords—**Flexible ac-transmission system (FACTS) device, inverterless converter, partial power conversion, power flow control,voltage compensation.**

I. INTRODUCTION

As the price of the fossil fuel keeps on growing in the last decades, the government and public people show greatinterest to the renewable energy applications. The fossil-fuelbased generation system is shifting to the renewable energybased generation one in the electric grid, which is promoted by the government in many countries [1]. The increasing penetration of renewable energy, the growing demand of the electrical power, and the aging of networks make it desirable to control the power flow in power-transmission systems fast and reliably[2]. On the other hand, as the rapid development of the industrial economy, soaring installation of the nonlinear loads greatly degrade the power quality of the grid. Reactive power variations and voltage fault such as voltage harmonics, voltage sag, and voltage surge occur occasionally, which increases the transmission losses and cause the nearby sensitive equipment to malfunction [3]. In order to meet the power quality requirement defined in the IEEE 519 [4] to avoid the large penalties and protect the nearby equipment, additional compensation devices
installation is inevitable.

Traditional offline optimal power flow control techniques, including setting the operating points of various generators, shunt VAR compensation, and load tap-changing setting, may not be the desirable solutions mainly because of the large reactive loop current which may cause in a meshed grid structure and also the slow response time due to the complex algorithm[1].

The unified power flow controller (UPFC), which is considered as the most powerful flexible ac-transmission system (FACTS) device, can be utilized to control the power flow in power-transmission system[6],[7]. The same structure applied in power-distribution system, which is named as unified power quality conditioner (UPQC), is designed to perform the compensation functions for voltage sag/swell, voltage harmonics, and reactive power[8]. The UPFC device has two inverter-type converters coupled with a common dc link. The series inverter injects a four-quadrant voltage with controllable magnitude and phase in series with the line to realize multiple functions such as power flow control and voltage compensation at the same time. However, the UPFC device needs a large energy storage element in the dc-link[5] part, which is usually the electrolytic capacitor with short lifetime[9]. As a result, it has problems when installed to the power system with high reliability requirements. In order to overcome the drawbacks, an improved device named distributed power-flow controller (DPFC)[5] is proposed based on the new distributed FACTS concept. The DPFC device, which has the same function as the UPFC, eliminates the common dc link between the shunt and series inverters. It has lower cost and higher reliability than the UPFC devices. Nonetheless, the DPFC device still has the large capacitors installed in both its shunt and series inverter, which means that the reliable issue has not been essentially solved. In the micro grid system, distributed structures based on the UPQC devices are discussed in[11]-[13]. The concept of these scenarios is to make use of the existing inverters which are connected to renewable energy sources or energy storage devices to implement the aforementioned functions. However, the applicable areas of these scenarios are apparently limited in the grid that has plenty of distributed generation devices. Thus, these solutions are hard to extend to most of the applications.

II.PARTIAL POWER CONVERSION DEVICE (PPCD)

The proposed PPCD circuit is derived from the push–pull forward dc-dc converter. Fig. 1(a) shows the schematic of the ac–ac push–pull forward converter where the input and output voltage is ac and the MOSFET S_1 and S_2 are replaced by two bidirectional switches. The transformer T_1 is a three winding transformer where the turns of two primary side and secondary side are nP_1, nP_2, and ns , respectively. The turn ratio N of T_1 is expressed as N = ns /n where nP = nP_1= nP_2.The coupling reference is pointed by "*." The advantage of the topology is that the energy in the leakage inductances Lk_1 and Lk_2 of T_1 can be absorbed and recycled by adding a clamping capacitor C_S . As a result, the voltage stress on S_1 and S_2 is limited. The final version of the PPCD circuit is derived by reforming the ac–ac push–pull forward topology circuit. As shown in Fig. 2(b), each bidirectional switch in Fig. 2(a) is realized by two separated IGBTs with antiparallel diodes. Thus, the connected IGBTs Q_2-Q_3 and Q_1-Q_4 can be replaced by the IGBT bridge type module, respectively which facilitates the high power application for this circuit. As a trade-off, two clamping capacitors Cs_1 and Cs_2 are required as shown in Fig. 1(b). In the final version, the output LC filter is moved from the secondary side of the transformer NS to both primary sides NP_1 and NP_2. As a result, the high-frequency harmonic components superposed onNP_1 and NP_2 are eliminated. The transformer, thus, is easier to design.

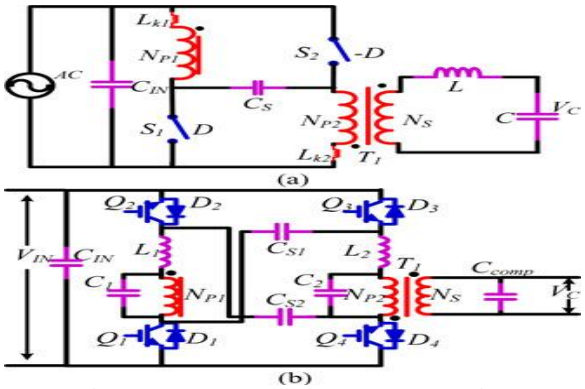

Fig.1 Evolution of a PPCD circuit. (a)Original ac-ac push-pull forward converter.(b) Final version of a PPCD circuit.

Pulse width modulation technique is implemented to generate the switching signals for the IGBT Q_1-Q_4 . The generation of the switching patterns depends on the different polarities of the input voltage, which is shown in Table I. When the input voltage V_{in} is positive during the operation, Q_1 and Q_3 are switched in high frequency, whereas Q_2 and Q_4 are normally ON. The gate signals of Q_1 and Q_3 in this case are complementary with additional enough dead time. The switching patterns are reversed when Vin is negative, which are also given in Table I.

mode	Input Voltage	Q_1	Q_2	Q_3	Q_4
(a)	"+"	High frequency switching	Normal on	High frequency switching	Normal on
(b)	"-"	Normal on	High frequency switching	Normal on	High frequency switching

The two circuits in Fig. 1 have the same voltage transfer characteristic which can be attributed to buck-type essentially. So the voltage gain analysis can be based on the circuit displayed in Fig.1(a). The duty ratio of the bidirectional switch S_1 is defined as D. The duty ratio of S_2 is defined as −D. The control range of D is [−1, 1] where "−1" means normal OFF and "1"means normal $_{ON.}$ The turn ratio N of T1 is expressed as N= ns /np where nP = nP_1 = NP_2 . The output voltage V_c of the circuit can be derived by applying the principle of inductor volt–second balance and using the small-ripple approximation; the result is displayed as follows:

$$V_C = V_{in} \cdot D \cdot N. \quad (1)$$

Assuming that the circuit is lossless, the input current is I_{con} and the output current is Ic ; the power rate of the ac–ac converter in the PPCD circuit is given as follows:

$$P_{rate} = \max\{_{VinIcon}\} = \max\{V_C I_C\} = \max\{ND V_C I_C\} = N V_C I_C = NPr \quad (2)$$

By defining the system power rate

$$P_r = V_{in} \cdot I_C, \quad (3)$$

The result of (2) shows that the power rate of the converter is $N \cdot P_r$. Typically, N varies from 0.1 to 0.5, which means that the converter is a partial power converter. The conclusion is the same for the transformer T_1 since it transfers all the power go through the converter.

II. SYSTEM MODELING AND CONTROL METHOD ANALYSIS FOR POWER FLOW CONTROL

In this section, the system model with PPCD for power flow control is derived. Based on this model, the available control range is given and then a minimum power transfer control strategy is proposed to control the power flow at the same time to minimize the power loss of the converter.

Fig. 2 shows the typical system configurations with the proposed PPCD. The converter is placed between the generation area and the load area. The voltages of the two areas are separated by a phase difference δ.

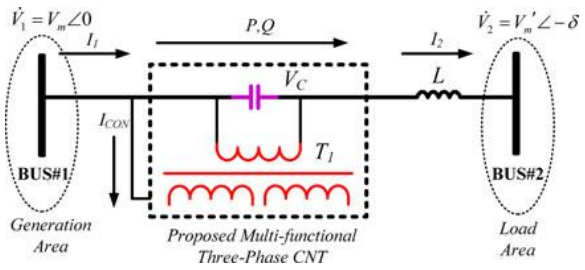

Fig. 2. Typical system configurations with the proposed PPCD for power flow control.

The original inductance of the transmission line is assumed to be L, where X_L represents its impedance. The PPCD injects a controllable compensation voltage V_c in series through the connection transformer T_1 to control the power

flow. The PPCD then can be considered as a controllable voltage source. The input energy of PPCD is drawn from the generation area and the input current is I_{con}. According to (2), the power rate of the system is P_r and the power rate of the converter is $N \cdot P_r$. Compared with the solution in Fig. 1 the ac–ac converters have the same partial rate N·Pr if the turn ratio N equals the tap ratio n in Fig. 1, while T_1 has the partial rate $N \cdot P_r$ compared to the full-rated transformer in Fig. 1. In order to make the analysis easier, the power loss of the transmission line and the PPCD is ignored in the analysis given in the following.

III. POWER FLOW CONTROL MODEL ANALYSIS

In this paper, the PPCD for power flow control is modeled . The system can be first modeled as Fig. 3(a) . The PPCD is represented by an ideal series voltage source Vc in series with the line impedance X_L. The voltage on BUS#1 and BUS#2 is given in (4) and (5), and the output voltage V_{OUT} satisfies(6).

$$V_1 = \sqrt{2}\, V_m \sin \omega t \tag{4}$$

$$V_2 = \sqrt{2}\, V_m \sin(\omega t - \delta) \tag{5}$$

$$V_{OUT} = V_1 + V_2 \tag{6}$$

In order to generate an appropriate voltage V_c to change power flow between the two area, by applying the DVQS voltage synthesis theory and using the even harmonic modulation (EHM) scheme [9], the duty ratio D of the ac–ac converter is given in the form of a dc component K_0 added a second harmonic component where the amplitude and phase are K_2 and ϕ_2 , respectively. It is expressed as follows:

$$D = K_0 + K_2 \sin(2\omega t + \phi_2) . \tag{7}$$

Substituting (4) and (7) into (1), the V_C can be calculated and given in complex form

$$V_C = r\sqrt{2}\, V_m \angle \Psi \tag{8}$$

$$r = N\sqrt{(K_0 - \frac{1}{2} K_2 \sin\Psi 2)^2 + (\frac{1}{2} K_2 \cos \Psi_2)^2} \tag{9}$$

$$\Psi = \arctan\left(\frac{\frac{1}{2} K_2 \cos \Psi_2}{K_0 - \frac{1}{2} K_2 \sin \Psi 2}\right) \tag{10}$$

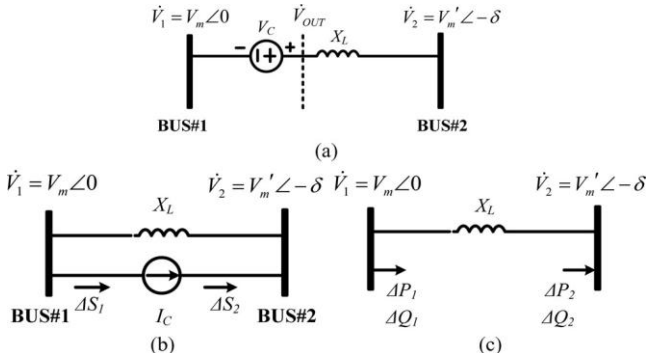

Fig. 3 Derivation of injection model for power flow control. (a) PPCD circuit being replaced by a voltage source. (b) Replacement of a voltage source by acurrent source. (c) Final injection model.

It should be noticed that because of the injection of second harmonic modulation signal, Vc consists of first and third components. In a symmetrical three-phase power system, the third harmonics can be naturally blocked and the expression for V_C is, thus, simplified.

In order to analysis the influence to the system after the compensation, an injection model for the system can be further obtained, which is shown in Fig. 3(b). The voltage source V_C is replaced by the current source Ic in parallel with the original line impedance X_l. The Ic satisfies the equation

$$I_C = \frac{Vc}{jXL} \tag{11}$$

The current sources I_C corresponds to the injection current after applying the power flow control, and the injection power ΔS_1 and ΔS_2 are expressed as

$$\Delta S_1 = V_1 * I_C = \Delta P_1 + \Delta Q_1 \tag{12}$$

$$\Delta S_2 = V_2 * I_C = \Delta P_2 + \Delta Q_2 \tag{13}$$

Further considering the effect of the converter current I_{con}, the final model are demonstrated in Fig. 3(c). The injection power ΔS_1 is modified to

$$\Delta S_1 = V_1 * I_C + V_1 * I_{con} = V_1 * I_C + V_c(\frac{Vc + V2 - V1}{jXL}) = \Delta P_1 + \Delta Q_1 \tag{14}$$

The corresponding incremental active power flow ΔP_1 , ΔP_2 and reactive power flow ΔQ_1 , ΔQ_2 can be derived from (12) and (13); the results are given in (14)–(17). As soon as all the losses are neglected, ΔP_1 is equal to ΔP_2

$$\Delta P_2 = \frac{rVm\ 'Vm}{XL} \sin(\delta + \psi) \tag{15}$$

$$\Delta Q_2 = \frac{rVm\,'Vm}{XL}\cos(\delta + \varphi) \quad (16)$$

$$\Delta P_1 = \frac{rVm\,'Vm}{XL}\sin(\delta + \varphi) \quad (17)$$

$$\Delta Q_1 = \mathrm{Im}\{V_1.(Ic)^* + Vc(\frac{Vc+V2-V1}{jXL})^*\} \quad (18)$$

The active power flow P_2 and reactive power flow Q_2 to the BUS#2 are the control targets. According to (14) and (15), the power flow control can be realized by changing parameters r and ϕ. Since r and ϕ are determined by dc value K_0 , amplitude of the second harmonics K_2 , and its phase ϕ_2 in duty ratio D, the power flow control can be realized by controlling the duty ratio D of its ac–ac converter with the installation of the PPCD.

IV.POWER FLOW CONTROL RANGE DERIVATION

As the duty ratio D has its range [−1, 1], the parameters K_0 and K_2 are constrained by the following equation:

$$|K_0| + |K_2| \leq 1. \quad (19)$$

The power flow control range of the PPCD can be derived by the analysis of (9), (10), (15), and (16). For example, in the original system without the PPCD, the active power and reactive power to BUS#2 is given by

$$P_L = \frac{Vm\,'Vm}{XL}\sin\delta \quad (20)$$

$$Q_L = \frac{Vm^2 - Vm\,'Vm\cos\delta}{XL} \quad (21)$$

Assuming that δ = 2◦, $V_m \approx V_{m.}$ Then, it has sinδ = 0.0349, cosδ = 0.9994, $P_L \approx 1$ p.u., and $Q_L \approx 0$ p.u. The turn ratio N of the connection transformer is set to 0.1, which means that the power rate of the transformer is 0.1 p.u. Then, three typical conditions are analyzed in the following with the corresponding control range graph plotted in Fig. 4.

1) $K_2 = 0$, $K_0 \in [-1\ 1]$: Under this condition, (9) and (10) are simplified to r = 0.1 and ϕ = 0. By varying K_0 , according to (15) and (16), it can be found that ΔP_2 will be always small but ΔQ_2 is changed a lot. This conclusion is true when δ is small enough, which is the normal condition for a transmission line. The maximum absolute values of ΔP_2 and ΔQ_2 are 0.10 p.u.and 2.52 p.u., respectively, when $K_0 = \pm 1$, which is shown in Fig.4.

2) $K_0 = 0$, $K_2 \in [-1\ 1]$, $\phi 2 \in [-\pi\ \pi]$: Under this condition,(8) and (9) are simplified to r = 0.05 and ϕ = ϕ2. Let $K_2 = LI \pm 1$; from (15) and (16), a maximum control range circle can be plotted in Fig. 4 by varying ϕ_2 . The maximum absolute value of ΔP_2 and ΔQ_2 is 1.43 p.u.

3) $K_0 = \pm 0.5$, $K_2 \in [-1\ 1]$, $\phi 2 \in [-\pi\ \pi]$: The control range of this condition is between the conditions 1 and 2. The approximate maximum absolute value of ΔP_2 is 0.72 p.u. and ΔQ_2 is 2.15 p.u.

From the previous three examples, it can be concluded that the parameter K_0 mainly affect the ΔQ_2 , while the parameter K_2 and ϕ_2 affect the ΔP_2 and ΔQ_2 at the same time. The overall control range is much larger than the original power flow between the two areas.

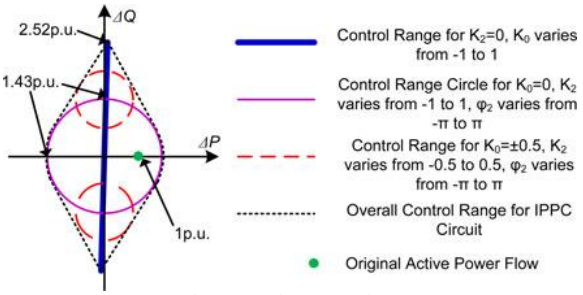

Fig.4. Control range of a PPCD for power flow control.

Relations between ΔP_2 , ΔQ_2 and $|\Delta S_2|$, (δ+ϕ) are displayed in Fig. 6(a), where $|\Delta S_2|$ is given as

$$|\Delta S_2| = \sqrt{(\Delta P2)^2 + (\Delta Q2)^2} = \frac{rVm\,'Vm}{XL} \quad (22)$$

Rewriting (22) and comparing with (9), the relations between $|\Delta S_2|$ and K_0 , K_2, ϕ_2 is derived

$$\frac{XL\,|\Delta S2|}{Vm\,'VmN} = \frac{r}{N} = \sqrt{(Ko + \frac{1}{2}K2\sin(-\varphi 2))^2 + (\frac{1}{2}K2\cos(-\varphi 2))^2} \quad (23)$$

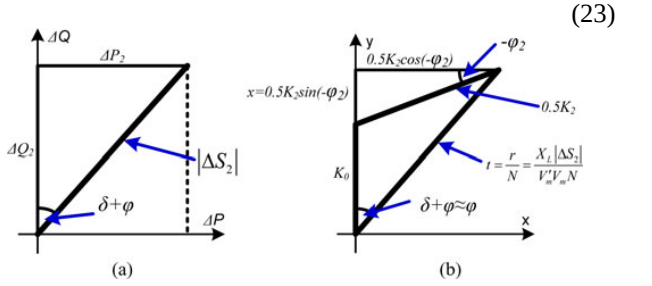

Fig. 5. Minimum power transfer control strategy derivation. (a) Geometric representation for $\Delta P2$ and $\Delta Q2$. (b) Geometric relationship between $\Delta P2$ and $\Delta Q2$ and $K0$, $K2$, $\phi 2$.

It is supposed that δ is small enough, which means δ+ϕ ≈ ϕ. Then, Fig. 5(a) can be modified to Fig. 5(b) referring to (22) and (9). Fig.5(b) demonstrates the geometry relationship between $|\Delta S_2|$, (δ+ϕ) and K_0 , K_2 , ϕ_2. From (3), it can be found that how much power the converter dealing with is decided by the maximum value of D, which is $|K_0| + |K_2|$. Assuming that $M(D) = |K_0| + |K_2|$, the minimum power transfer is achieved when M(D) reaches its minimum value.

The function M(D) can be rewritten to (24), where the definition of the variables x and t are given as

$$M(D) = |K_2| + |K_0| = \sqrt{(t\sin(\delta+\varphi))^2 + x^2} + |t\cos(\delta+\phi) - x| \quad (24)$$

$$x = \frac{1}{2}K2\sin(-\varphi 2)) \quad (25)$$

$$t = \frac{XL\,|\Delta S2|}{Vm\,VmN} = \sqrt{(Ko + \frac{1}{2}K2\sin(-\varphi 2))^2 + (\frac{1}{2}K2\cos(-\varphi 2))^2}$$

(26)

Differentiate (24) to find the minimum value of M(D); the results are as follows

$$\text{Min}\{M\} = \sqrt{3}t\sin(\delta+\varphi) + t\cos(\delta+\varphi), \text{when}(\delta+\varphi) < 60^0$$

$$2t, \text{when}\ (\delta+\varphi) > 60^0$$

These results are achieved under the following condition

$$x = \frac{t}{\sqrt{3}}\,t\sin(\delta+\Psi)$$

$$\Rightarrow K0 = t\cos(\delta+\phi) - \frac{t}{\sqrt{3}}\,t\sin(\delta+\Psi)$$

$$K_2 = \frac{4}{\sqrt{3}}\,t\sin(\delta+\Psi), \phi_2 = -30\circ, \quad \text{when}\ (\delta+\phi) < 60^0$$

$$x = t\cos(\delta+\phi) \Rightarrow K_0 = 0, K_2 = 2t,$$

$$\phi_2 = -(\delta+\phi), \text{when}\ (\delta+\phi) \geq 60\circ.$$

A more detail calculation can be presented to show how to implement the proposed control strategy. Assuming that in the system, as shown in Fig. 2, the nominal voltage on both sides is 110 kV and the line inductance L is 10 mH. The phase shift before the compensation is 2◦. Calculated, original active power flow is 134MW. Set the turn ratio N of T_1 to 0.1. It is supposed that the required increment active power ΔP_2 and reactive power ΔQ_2 are 50 MVA and 50 MVA, respectively; referring to the definition in (26), it has $\delta+\phi = 45\circ$, t = 0.367. According to (26), the duty cycle D can be given as K_0 = 0.055, K_2=0.3, $\phi_2 = -30\circ$,D=0.055+0.3sin(2ωt−30◦). Since the power rate of the converter is 0.1p.u., the output power of the converter at this time will be (0.055+0.3)·0.1p.u.=0.0355p.u., which is much less than the rated power of the system.

The operation process of the PPCD circuit is given as follows. During the operation, the PPCD will detect the instant power flow and also receive the power flow command from upper side control center. Required incremental active power and reactive power are generated by internal processor, and then, the duty cycle is calculated out based on the command and send to the converter. The aforementioned method is essentially an offline optimal control scheme which widely exists in the power flow control area of the grid.

V. VOLTAGE COMPENSATION METHOD DEVELOPMENT AND CLOSED-LOOP CONTROL ANALYSIS

The proposed PPCD is also designed to handle the voltage problems in the power distribution system. In this section, the system configuration for voltage compensation is given. Under this configuration, a simple closed-loop control method is realized with the control block diagram displayed, which shows that the system is easy to handle by applying the conventional proportional-integral-derivative (PID) controller.

Fig.6 shows the system configuration for voltage compensation. V_{in} is the voltage on point of common coupling (PCC),which is distorted by other disturbance sources. For example,Vin consists of a fundamental component V1 with its amplitude V_m and a fifth harmonic component V_5 with its amplitude V_{5m} and phase ϕ_5 as follows:

$$V_{in} = Vm\sin\omega t + V5m\sin(5\omega+\phi_5) \quad (27)$$

The system output is a critical load that requires pure sine input voltage. The expected bus voltage is V_{out} with its rated voltage V'_m. The PPCD is placed between power grid and load. The system shown here is similar with the system for power flow control shown in Fig.2; thus, the output voltage of PPCD is the same as (1), while Vout is expressed in the system

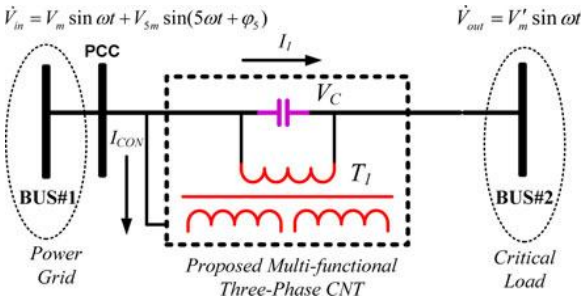

Fig. 6. Typical system with a PPCD circuit for voltage compensation

A. Voltage Compensation Method Analysis

Take the fifth harmonics elimination and fundamental voltage regulation functions for example. In order to eliminate the fifth harmonic component and regulate the fundamental component to desired Vout , by applying the DVQS voltage synthesis theory and using the EHM scheme[9], the duty ratio D is given in the form of a dc component K_0 added to a fourth harmonic component with its amplitude K_4 and in phase with the fifth harmonic component in V_{in} , which is expressed as follows:

$$D = -[K_0 + K_4\cos(4\omega t + \phi_5)] \quad (28)$$

Substituting (27) and (28) into (1), V_{out} can be, then, derived as

$V_{out} = (V_m \sin \omega t + V_{5m} \sin(5\omega t + \phi_5)) \times (1 - N(K_0 + K_4 \cos(4\omega t + \phi_5)))$

$= a_1 \sin\omega t + a_5 \sin 5\omega t + a_3 \sin 3\omega t + a_9 \sin 9\omega t$ (29)

Where $a_1 = (1 - NK_0)V_m - \frac{N}{2} K_4 V_{5m}$, $a_3 = \frac{N}{2} K_4 V_m$, $a_5 = (1 - NK_0)V_{5m} - \frac{N}{2} K_4 V_m$, and $a_9 = -\frac{N}{2} K_4 V_{5m}$.

The goal of voltage compensation is to maintain the amplitude of V_1 to Vm' _ and eliminate the amplitude of V_5 to zero. Then, it has

$a_1 = (1 - N K_0)V_m - \frac{N}{2} K_4 V_{5m} = V'_M$ (30)

$a_5 = (1 - N K_0) V_{5\ m} - \frac{N}{2} K_4 V_m = 0$ (31)

In practice, it satisfies $V_{5m} \ll V_m$, $N < 1$, $K_0 < 1$, $N \cdot K_0 \ll 1$. So (30) and (31) can be simplified.

$a_1 = (1- N K_0) V_m = V'_M$ (32)

$a_5 = V_{5m} - \frac{N}{2} K_4 V_m = 0$ (33)

In this two simplified (32) and (33), the control of regulating the fundamental component and eliminating the harmonic components are decoupled. The fundamental component of V_{out} can be adjusted to certain value V_m by changing K_0 , while the fifth harmonic can be eliminated to zero by changing K_4 . It means that, despite of the variations in V_m and V_{5m}, a pure sine voltage with desirable amplitude can be synthesized by regulating the duty cycle D of the PPCD circuit. Generally, in a typical three-phase power distribution system, low-frequency odd-order harmonics such as 5^{th}, 7^{th}, 11^{th}, and13^{th} are the main harmonics. By utilizing the same method mentioned previously, the 4^{th}, 8^{th}, 10^{th}, and 14^{th} even-order harmonics are added into the modulation wave of the duty cycle D to eliminate the corresponding voltage harmonics in the system. Similar with the power flow control, the voltage compensation control range is also limited by the duty ratio D, which is expressed as

$$|K_0 | + |K_4 | + |K_8 | + \cdots \leq 1. \quad (34)$$

However, it is difficult to plot the control range as Fig. 5 shows for fundamental voltage regulation and harmonics elimination, especially when the system contains various orders of harmonics. According to (1) and (29), an example can show the maximum control range: If N = 0.3, the maximum amplitude of fundamental voltage is ±0.3·Vm,while the maximum amplitude of harmonic voltage is ±0.15·Vm.

B. Closed-Loop Control Realization

A control architecture, which is based on the parallel form of a DVQS-applied converter, is proposed in [4] and [15] to realize closed-loop control for power factor correction and current harmonic filtering. SRF control theory is employed in the architecture to extract the fundamental component and also the harmonic components in the current waveform. In a similar way,closed-loop control for the PPCD is proposed to realize fundamental voltage regulation and harmonics elimination function.The control architecture shown in Fig. 7.

Because the control of the two main functions are decouple due to former analysis, the control architecture has several decoupled control loop including the harmonics elimination loops for each order harmonics and the voltage regulation loop, which is displayed in Fig.7. In the controller part of the architecture, the three-phase voltage after the compensation V_{OUTk} is sampled first. In order to extract the amplitude of each nth harmonics or fundamental component in V_{OUTk} , Park's transformation is introduced to transform the output "abc" voltage to the "dq" voltage in each frequency order.This method assumed that the voltage is almost balance. After the extraction, digital low-pass filters are employed to eliminate ac components from the results. The remaining dc components correspond to the amplitude of each order harmonics and the fundamental component in $V_{OUTk.}$

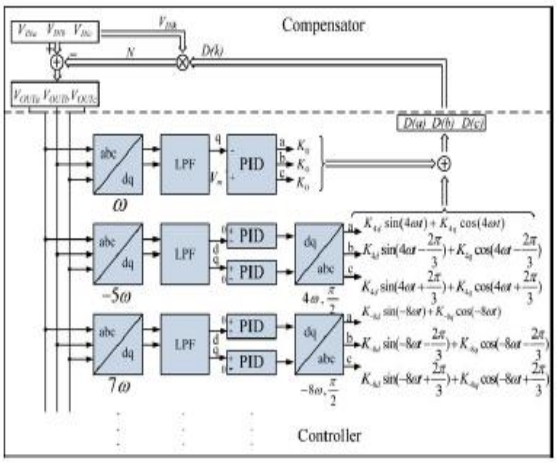

Fig.7.Closed loop control architecture within harmonics elimination & voltage regulation

Following that, the outputs from the filters are compared with the references. For the fundamental voltage regulation loop, the value from "d"-axis should always be zero and the "q"-axis value is compared with reference V'm. For the harmonics elimination loop, the value from both "dq" axes is compared with zero. Taking the reverse-feedback mechanism into account, the input of PID compensator should be connected as Fig.7 shows. After the comparison, the differences are sent to PID compensators that are utilized to generate the coefficient of D in "dq" form. Then, the coefficient from harmonics loop in "dq" form is transformed to "abc" form by applying Ipark's transformation. It should be noticed that particular evenorder harmonics are required in duty cycle D to eliminate the corresponding odd-order harmonics in V_{OUTk} . Thus, Ipark's transformation matrixes with special frequency and angle are applied in the architecture, which is also given in Fig. 7. Finally, the coefficients in "abc" form and the output from fundamental voltage loop are combined together to be the modulation waveform of D which is sent to each phase PPCD circuit.

Relation of the duty ratio D in the three-phase system ,input voltage and the output voltage V_{OUTk} (k = a,b,c) can be then derived as

$$V_{OUTk} = \begin{bmatrix} V_{OUTa} \\ V_{OUTb} \\ V_{OUTc} \end{bmatrix} = \begin{bmatrix} V_{INa} \\ V_{INb} \\ V_{INc} \end{bmatrix} \cdot \left(1 - \begin{bmatrix} D(a) \\ D(b) \\ D(c) \end{bmatrix} N \right) \quad (28)$$

With the injection of 4th, 8th, 10th, and 14th even harmonics with proper amplitude and phase in the modulation signal, a series of 5th, 7th, 11th, and 13th odd harmonics which has the same amplitude and out phase with the existing harmonics is generated by the compensator and counteracted the existing 5th, 7th, 11th, and 13th harmonics, only left are the fundamental component and residual higher frequency harmonics. The amplitude of the fundamental component is controlled by setting the value of K_0 . So the problems such as the voltage sag, the voltage surge, and the voltage undergoing can be handled at the same time.

VI. SIMULATION AND EXPERIMENTAL VERIFICATIONS

In order to verify the effectiveness of the proposed PPCD, the system in Figs.2 and 6 with the proposed converter is simulated in MATLAB/Simulink. A same power rate prototype is assembled to compare with the simulation for voltage compensation

A. POWER FLOW CONTROL SIMULATION

The simulation system configuration for power flow control is the same as Fig. 3 shows. The specification of the system is V1 : 110 kV, V_2 : 110 kV, and L = 10 mH. The phase shift between the two bus is δ = 2◦. The PPCD circuit is the same as Fig. 1(b) shows, where the specification is fs: 10 kHz, C_{in} : 5 μF, C_1, C_2, Cs_1, Cs_2: 10μF, L_1 , L_2 : 1 mH, and C_{comp}: 1μF.

Calculating with (20), the original active power flow of the system Pout is 134 MW. The original reactive power flow Qout of BUS#2 is −2.3 MVAR. Fig. 8 displays the system power flow change by utilizing the PPCD circuit. The settings of the control variables D are also given to indicate the instantaneous power transferred through the PPCD circuit. As shown in Fig.9, The PPCD is running in standby mode from 0 to 0.2 s. At this time, K_0 and K_2 is zero. The active power flow Pout remains unchanged, while the reactive power Q_{out} slightly decrease to −19 MVAR. K_0 changes to 0.5 at t = 0.2 s. At this time, Q_{out} increases to 193 MVAR, but Pout just increases to 143 MW, which shows that K_0 mainly affects reactive power. At t = 0.4 s, K_0 becomes 0 and K_2 increases to 0.5.

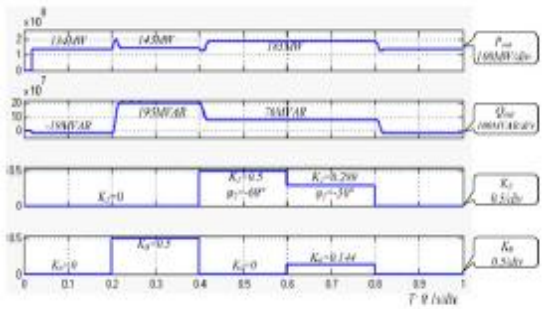

Fig.8.System power flow change and control variables setting during power flow simulation

From the Pout and Q_{out} waveform, it can be found that both of them are changed. It proves that Pout and Q_{out} can be both determined by varying K_2 and ϕ_2 . During this period, M(D)0.4 = 0.5, Pout = 185MW, Q_{out} = 76 MVAR. At t = 0.6 s, the minimum power transfer strategy is implemented on the PPCD. The Pout and Q_{out} have not been changed at this moment, but different values of K_0 , K_2 , and ϕ_2 are used. It has M(D)0.6 = $|K_2|+|K_0|$ = 0.433 < M(D)0.4 , which means that the PPCD circuit deals with less power during this time than the time from 0.4 to 0.6 s. The result shows the effectiveness of the minimum power transfer strategy.

Fig.9 shows the step change waveform of the system active and reactive power flow when the PPCD begins to operate. It can be found that at the time 0.4 s, a compensation voltage Vc is injected by the PPCD. Vc consists of fundamental component as well as the third-order harmonics. The system active and reactive power flow is then changed greatly

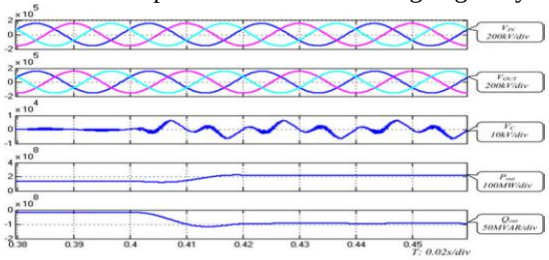

Fig.9.Step change demonstration of system P&Q after applying a PPCD circuit.

B. VOLTAGE COMPENSATION SIMULATION

The simulation system configuration for voltage compensation is the same as Fig. 2 shows. The specifications of the system are given by V_{in} : 190–250 V; V_{out} : 220 V; V_{line} : 380 V; P_{out} : 30 kW; fs: 10 kHz; C_{in} : 5μF; C_1 , C_2 , C_{S1} , C_{S2} : 10 μF; L_1 , L_2 : 1 mH, and C_b : 1 μF. The system is designed to eliminate 5th,7th, 11th, and 13th harmonics with 15% total harmonic distortion(THD) and deals with the 15% voltage sag and voltage swell taking place in Vin .

Fig.10 shows the simulation result of the proposed system during the voltage sag. The input line voltage V_{acIN} fells to 321.5V during the simulation, which becomes 85% of the rated voltage. The PPCD circuit in each three phase injects a fundamental voltage in phase with the input voltage. As a result, the output line voltage V_{acOUT} remains at rated voltage, which is 379.8 V as shown in Fig. 10. The THD of V_{acOUT} is slightly increased because of low-frequency harmonics caused by switching. This problem can be solved by further applying the harmonics elimination function which is shown in the following.

Fig.11 demonstrates the operation of the harmonics elimination function. 4.8% of the 5th, 7th, 11th, and 13th harmonics are generated in the input voltage V_{acIN}. Thus, its THD is 9.546% according to the calculation. With the operation of the PPCD circuit, the THD of the output voltage V_{acOUT} is reduced to 3.639% which is much smaller than the input.

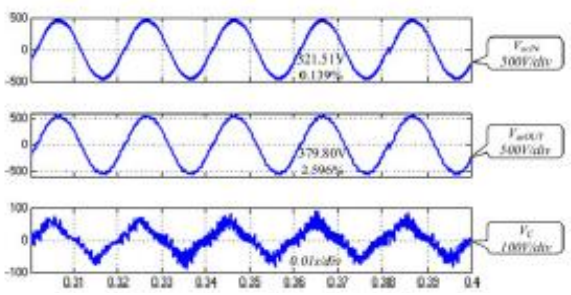

Fig.10.Simulation result of a system during voltage sag

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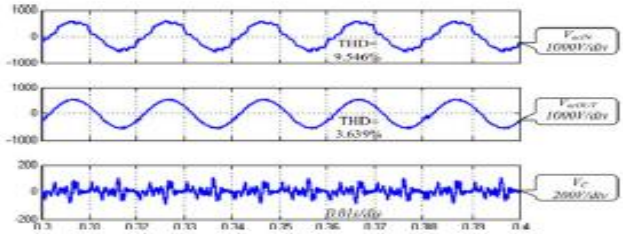

Fig.11.Simulation result of harmonics elimination

Fig. 12 shows the fast Fourier transform (FFT) analysis of the V_{acIN} and V_{acOUT}. It is clear that the 5th, 7th, 11th, and 13th harmonics are all greatly reduced by the operation of the compensator. Although the output voltage still cannot be considered as the pure sine because some uncontrolled harmonics such as 15th, 17th, and 19th order are slightly increased due to the switching operation of the PPCD circuit. The performance can be further improved by adding more control loops in the PPCD circuits to eliminate the higher order harmonics.

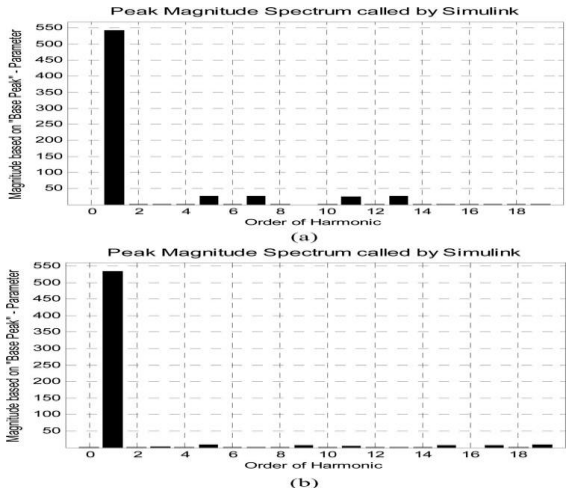

Fig.12.Harmonics contents comparison between input and output voltage (a) FFT analysis of V_{acIN}.(b) FFT analysis of V_{acOUT}

VII. PROTOTYPE DEMONSTRATION

A prototype is designed to verify the voltage compensation function. The specification of the prototype is the same as the voltage compensation simulation model mentioned in Section B. Fig. 13(a) demonstrates the 30-kW prototype. It consists of the digital control board, the PPCD direct ac–ac circuit, the connection transformer, and the breaker. The function of regulating the fundamental voltage is demonstrated by varying the input voltage using an auto-transformer. In order to verify the function of eliminating the harmonic components, an additional harmonic generation circuit is designed to generate the harmonics. The schematic of the circuit is shown in Fig.13(b). Inductors and diode rectifier are used to simulate the impedance of the transmission lines and nonlinear load in the experiment. The inductance of the inductor is 1.8 mH. The THD of the voltage on PCC can be adjusted by altering the resistor. In the experiment, the total load is 15 kW.

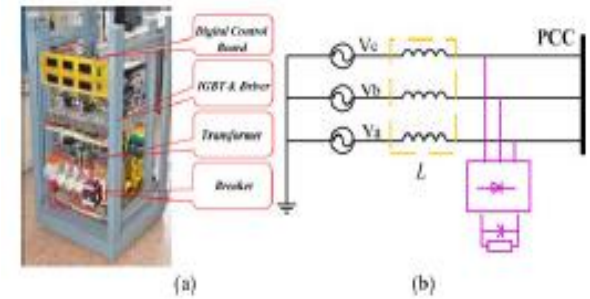

Fig.13 .30kW prototype for voltage compensation (a) Prototype. (b) Schematic of a harmonic generation circuit

Fig.14 shows the experimental results of fundamental voltage regulation. From the results, it can be found that despite the variations in the input voltage, the fundamental value of output voltages such as V_{bcOUT} and V_{abOUT} are maintained to about 380 V_{rms} . The THD of the output voltage is smaller than the simulation shows. The reason is that the high-frequency harmonics caused by switching is damped by the wire resistance in the circuit.

Waveform shown in Fig.15(a) demonstrates the harmonics elimination function and fundamental voltage regulation at the same time. The fundamental RMS value of V_{abIN} is 345.75 V and the THD of V_{abIN} is 8.407%, while the fundamental RMS value of V_{abOUT} is 380.64Vand the THD of V_{abOUT} is 2.134%.Fig. 15(b) displays the results of Fourier analysis for both input and output voltage. It can be found that 5th, 7th, 11th, and 13th harmonics are decreased greatly, while the 15th, 17th, and other uncontrolled harmonics are not increased significantly

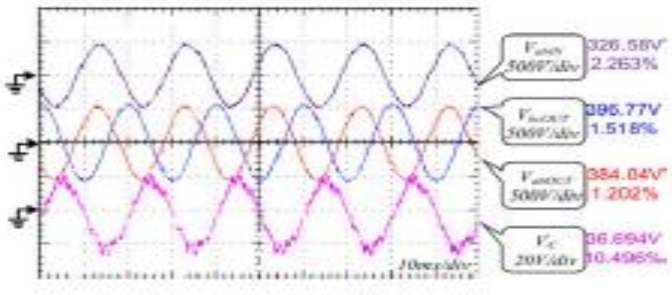

Fig.14.Experimental results of fundamental voltage regulation

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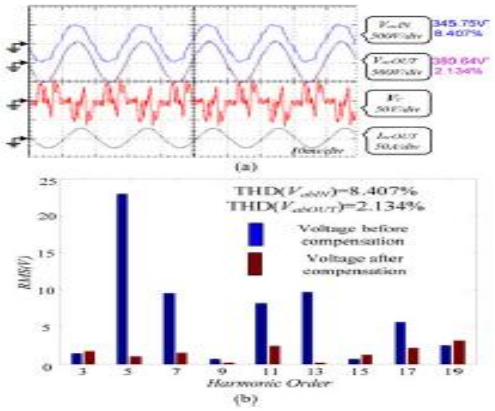

Fig. 15. Experiment results of harmonic elimination. (a) Waveform for harmonics elimination function. (b) Fourier analysis for input and output voltage

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