High Step-Up Resonant Push-Pull Converter for Stationary Plasma Thruster

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***Abstract*— In this paper, A step -up resonant push-pull converter is proposed. Conventional push-pull converter do not have high efficiency because of high switching losses by hard switching and transformer losses by high turns ratio of the transformer. In the proposed converter the load can be powered from solar-cell, a battery etc.. The power conversion circuit consist of four active switches, By adjusting the duty ratio of the active switch, the voltage regulation at the output can be made and it also makes the converter operates under resonant condition over a wide input voltage range. The circuit operation is described in detail with the theoretical analysis and computer simulation using MATLAB SIMULINK.**

Keywords—component; formatting; style; styling; insert (key words)

I. INTRODUCTION

Isolated dc-ac inverters have been widely used in domestic and industry applications. Some of those are powered by low-voltage sources such as fuel cells and solar cells. In these cases, the output voltage of the front –end converters has to be higher than a peak of sinusoidal output of the inverter. Therefore in order to interface fuel cells and solar cells to a high-voltage dc bus, high step-up dc-dc converters with high efficiency, high conversion ratio and very low input current ripple are required. Characteristics of the high step-up converters are very different from those of step-down converters. Input current ripple, input current stress and high-voltage conversion ratio are usually more important rather than zero-voltage switching (ZVS) of primary switches, output current ripple, conduction loss of rectifying stage etc. [1, 2]. Reverse–recovery problem of the output rectifying diodes is also an important issue since it causes a significant efficiency reduction as well as severe electromagnetic interference because of the high output voltage [2–4]. An inductive output filter is undesirable since the inductor is a bulky and expensive component because of high-voltage stress on this inductor and rectifying diodes. Therefore current-fed topologies based on boost converter [1, 5, 6] have been applied in the high step-up dc–dc converters.

Conventional current-fed push–pull converter [8] and its key waveforms are shown in Fig. 1. The converter has advantages such as high-voltage conversion ratio, low input current ripple and low conduction loss of switches. It is also recognised that

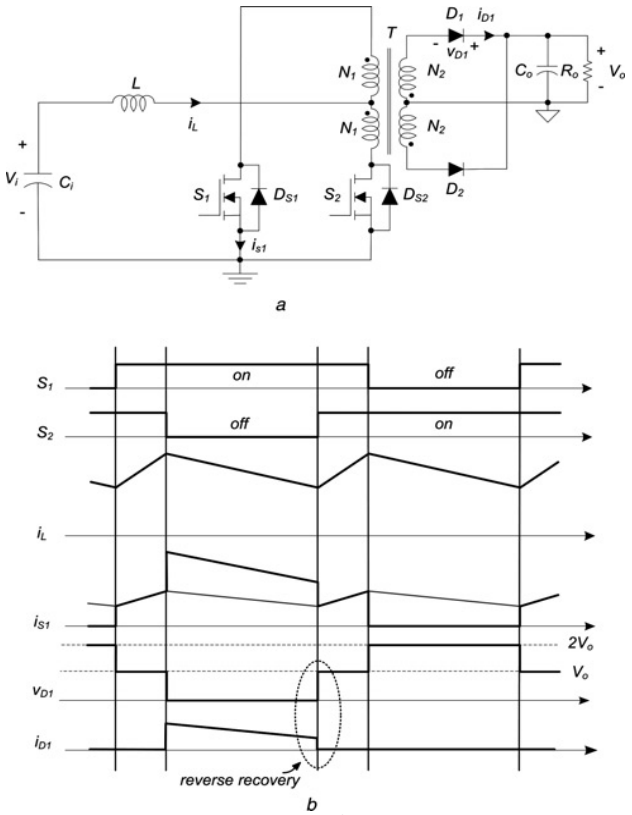


Fig. 1 Conventional current-fed push–pull converter
(a) Current-fed push–pull converter
(b) Key waveforms

flux unbalance is not a serious problem because of the high-impedance current-fed inductor feeding the push–pull transformer centre tap [7]. However, the converter has several problems such as voltage spikes of switches resulting from leakage inductance of a transformer, high-voltage stress and reverse–recovery problem of the rectifying diodes and low power conversion efficiency [8]. Also, since the duty ratio of the converter must be .0.5, its operating range of input voltage is relatively narrow. In recent years, some modified current fed converters have been presented to solve aforementioned problems. One of them is a ZVS clamping-mode current fed push–pull converter [9]. Its active-clamp circuit clamps a surge voltage of switches and recycles the energy stored in leakage inductance. Moreover, the converter can be allowed to operate at the duty ratio ,0.5, hence it can be suitable for wide input voltage applications. However, although this converter can achieve ZVS of switches, ZVS does not improve the efficiency sufficiently because the energy stored in output

capacitances of switches is small in low input voltage and ZVS condition requires relatively large leakage inductance or an additional inductor causing additional loss. Another approach, an active-clamp current-fed full bridge converter [1], is more novel and has high conversion ratio, soft switching of all switches and high efficiency. However, this converter only operates at duty ratio .0.5 and its control circuit is very complex because of a gate driving of an additional active-clamp switch.

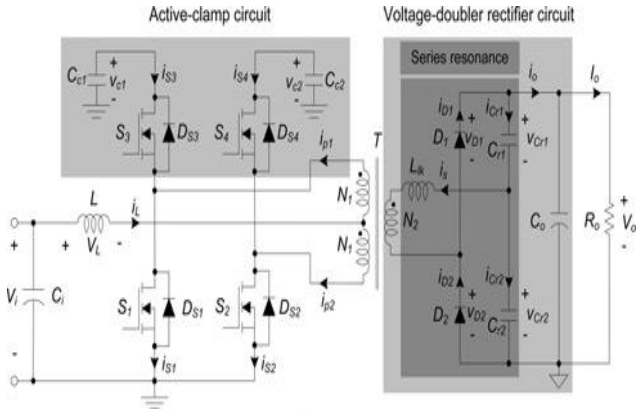


Fig. 2 Schematic of the proposed converter

A high-efficient current-fed push–pull converter shown in Fig. 2 is proposed in this paper. The proposed converter utilises LC resonance to provide a soft switching such as the quasi-resonant converters [10–12]. The quasi-resonant converters achieve the soft switching at the sacrifice of the conduction loss. Unlike the quasi-resonant converter in [11], the proposed converter has low conduction loss in primary side, since the input current is distributed in both the main and primary switches has low on resistance by reducing the voltage across the primary switches ,about 1.5 times the maximum input voltage. Although the proposed converter is structurally similar to the ZVS clamping-mode current-fed push–pull converter [9] except for the output rectifier, the analysis and design of the proposed converter are very different. Without additional devices, loss in the output rectifier during the commutation interval is reduced since the output diodes can commutate softly without the reverse–recovery problem. The voltage doubler rectifier doubles a conversion ratio and the voltage stress on rectifying diodes is confined to an output voltage [13]. Reduced turns-ratio of the transformer and soft switching of rectifying diodes can increase the overall efficiency. The advantages in comparison with the ZVS clamping-mode current-fed push–pull [9] or the active clamp current-fed full-bridge converter [1] are higher voltage conversion ratio, soft switching of rectifying diodes and wide input voltage range. In particular, an additional distinguished feature is that the input ripple current of the proposed converter is extremely low at the duty ratio around 0.5.

II. CIRCUIT DESCRIPTION AND STEADY STATE ANALYSIS

The operation of the proposed converter shown in Fig. 2 is analysed. A PWM controller regulates an output voltage V_o by adjusting a duty ratio D like buck or boost converter, except that two equal and adjustable width, 180 degree out of phase pulses are supplied to drive main switches S_1 and S_2.Auxiliary switches S_3 and S_4 are driven complementarily with S_1 and S_2, respectively. Since magnetizing inductance of the transformer is large and bidirectionally excited, a magnetizing current is nearly zero. Therefore, magnetizing inductance can be neglected to simplify the analysis and the transformer is modelled as an ideal transformer T and a Leakage inductance L_{lk}. A boost inductor L is connected to the transformer's centre tap. An active-clamp circuit is composed of clamp capacitors C_{c1} and C_{c2} and auxiliary switches S_3 and S_4. A voltage-doubler rectifier is composed of rectifying diodes D_1 and D_2 and resonant capacitors C_{r1} and C_{r2}. In order to analyze the operation, several assumptions are made.

1. The switches S_1, S_2, S_3 and S_4 are ideal except for their body diodes D_{S1}, D_{S2}, D_{S3}, and D_{S4}.
2. Vo is constant during one switching period Ts because the capacitance of an output capacitor C_o is sufficiently large.
3. C_{c1} is equal to C_{c2} and C_{r1} is equal to C_{r2} to achieve a symmetric operation.
4. Capacitances of C_{c1} and C_{c2} are sufficiently large so that ripple components on C_{c1} and C_{c2} are negligible.

The proposed converter can operate in two regions. When D is smaller than 0.5, the converter operates in a non overlapping region. In this region, both of the main switches are simultaneously in off-state during some intervals. When D is .0.5, the converter operates in an overlapping region. In contrast with the non-overlapping region, both of the main switches are in on-state during some intervals. The circuit is usually designed not to remain in one region throughout the full range of input voltage. Rather, it is designed to move from the non overlapping region to the overlapping region, as the input voltage shifts from its maximum to minimum specified value. This permits proper operation throughout a larger range of input voltage rather than its operation which remains within one region throughout the entire range of input voltage.

A. Principle of operation for D < 0.5

Figs. 3 and 4 show three topological modes during a half period and their theoretical waveforms, respectively. In the Non-overlapping region, six topological modes exist within Ts. However, it is necessary to describe only three of them, Since the remaining three modes are analogous. Theoretically, both of the voltages across C_{c1} and C_{c2} are equal to V_C during one switching period since the Converter is symmetrically operated and the capacitances of C_{c1} and C_{c2} are sufficiently large. Prior to Mode 1, the primary current ip1 flows through S_3 and i_{p2} flows through S_2.

Mode 1 [t_0, t_1]: At t_0, S_2 is turned off. i_{S2} that had been flowing through S_2 flows through D_{S4} as shown in Fig. 4. After a short dead time, S_4 is turned on while its body diode D_{S4} is still conducting. Since all voltages across windings are zero and V_C is higher than V_i, i_L decreases linearly as

$$i_L(t) = i_L(t_0) - \frac{V_C - V_i}{L}(t - t_0) \quad (1)$$

Since the sum of the magneto-motive force of all windings is zero, i_L is equally divided and flows into S_3 and S_4 as follows

$$i_{S3}(t) = i_{S4}(t) = -\frac{i_L(t)}{2} \quad (2)$$

Before the end of this mode, S_3 is turned off and its body diode D_{S3} is conducted during the short dead time.

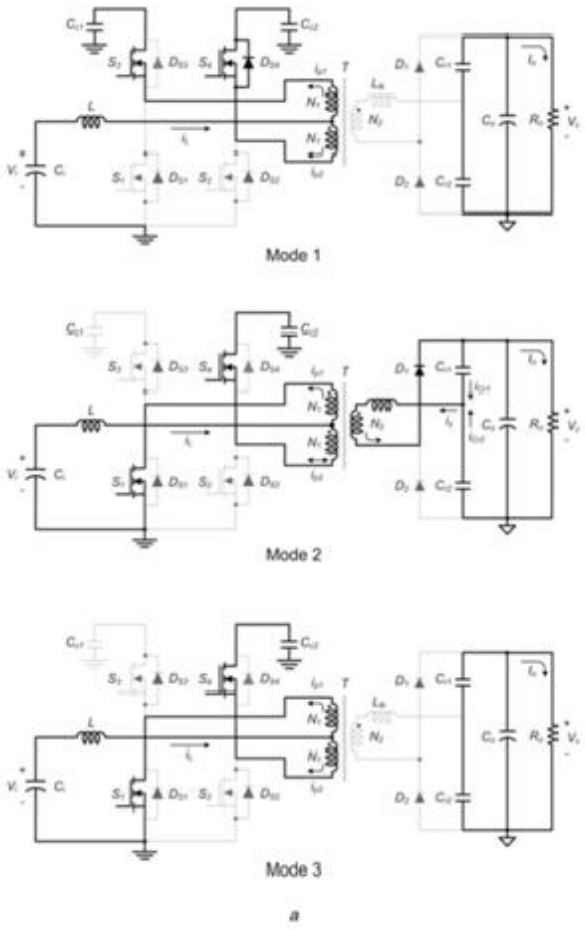


Fig. 3 Topological modes and waveforms for D< 0.5

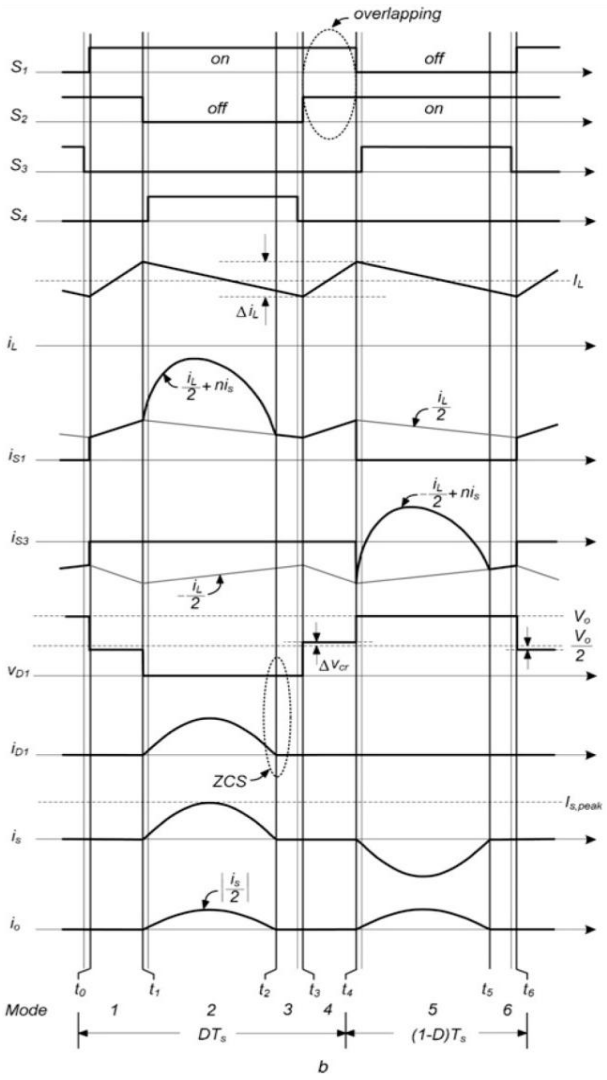


Fig. 4 Theoretical Waveforms of the Proposed Converter

Mode 2 [t_1, t_2]: At t_1, S_1 is turned on. The voltage at transformer centre-tab is 0.5 V_c which is lower than V_i. As shown in Fig. 4, i_L increases linearly as

$$i_L(t) = i_L(t_1) + \frac{V_i - .5V_c}{L}(t\text{-}t_1) \quad (3)$$

The voltage across L_{lk} is the difference between the secondary winding voltage and the resonant capacitor voltage V_{Cr1} and the input power is transferred to the load through the transformer. Since D_1 has been conducted, L_{lk} resonates with C_{r1} and C_{r2} while the secondary current is flows. The state equations can be written as

$$L_{lk}\frac{di_s(t)}{dt} = nVc - v_{Cr1}(t) \quad (4)$$

$$V_0 = v_{Cr1}(t) + v_{Cr2}(t) \quad (5)$$

$$i_s(t) = C_{r1}\frac{d_{Vcr\,1}}{dt} - C_{r2}\frac{d_{Vcr\,2}}{dt}$$

$$= C_r\frac{d}{dt}v_{Cr1}(t) \quad (6)$$

where turns-ratio n of the transformer and the effective resonant capacitance C_r are given by

$$n=\frac{N_2}{2N_1} \qquad C_r = C_{r1} + C_{r2} \tag{7}$$

From (4) to (6), V_{Cr1} and is are obtained as

$$v_{Cr1}(t)=nVc-(nVc- v_{Cr1}(t_1)) * \cos w_r\ (t-t_1) \tag{8}$$

$$i_S(t) = \frac{nVc - v_{Cr1}(t_1)}{z_r} \sin w_r\ (t-t_1)$$

$$= I_{s,\,peak} \sin w_r\,(t-t_1) \tag{9}$$

where $I_{s,\,peak}$ is the peak value of is, and the angular resonant frequency v_r and impedance Z_r of the resonance are given by

$$Z_r = \sqrt{\frac{L_{lk}}{C_r}} \qquad w_r = \frac{1}{\sqrt{L_{lk}C_r}} \tag{10}$$

Since C_{r1} and C_{r2} have the same capacitances, relations among the currents of the secondary side are as follows

$$I_{Cr1}(t)= - i_{Cr2}(t) = 0.5\, i_s(t)= i_0(t) \tag{11}$$

The sum of the magneto-motive forces of all windings is zero and the sum of the primary currents is i_L as follows

$$N_1 i_{p1}(t) - N_1 i_{p2}(t) - N_1 i_s(t) = 0 \tag{12}$$

$$i_L\,(t) = i_{p1}\,(t) + i_{p2}\,(t) \tag{13}$$

Thus, the switch currents are obtained as

$$i_{s1}\,(t) = i_{p1}\,(t) = \frac{i_L\,(t)}{2} + n\, i_s\,(t) \tag{14}$$

$$i_{s4}\,(t) = -i_{p2}\,(t) = - \frac{i_L\,(t)}{2} + n\, i_s\,(t) \tag{15}$$

Mode 3 [t_2, t_3]: At t_2, i_{D1} becomes zero and i_L still increases as shown in Fig. 4. The current i_L is equally divided and flows into S_1 and S_4 as

$$i_{s1}\,(t) = - i_{s4}\,(t) = \frac{i_L\,(t)}{2} \tag{16}$$

Since the resonance among C_{r1}, C_{r2}, and L_{lk} is terminated at t_2, D_1 can be turned off softly at t_3 whereas i_{D1} is zero.

The zero-current turn-off switching (ZCS) of D_1 removes its reverse–recovery problem. Operations of Modes 4, 5 and 6 during the remaining half period are analogous to the operations of Modes 1, 2 and 3, respectively. The average value of i_o during the half period is the load current Io as follows

$$\frac{2}{T_s}\int_{t_1}^{t_2} \frac{I_{s,peak}}{2} \sin(w_r\,(t-t_1))dt = I_0 \tag{17}$$

Thus, from (9) and (17), $I_{s,peak}$ is obtained as

$$I_{s,peak} = \frac{nV_c - V_{cr\,1}(t_1)}{z_r} = \frac{\pi w_r I_0}{w_s} \tag{18}$$

where w_s is an angular switching frequency. From (8), the average value of V_{Cr1} during a period is NV_C. Therefore from (18), ΔV_{Cr} in Fig. 4 is a function of load current as $\frac{\pi z_r w_r I_o}{w_s}$. From the mode analysis, the volt second balance law of L during the half period provides the relation between V_i and V_C as follows

$$(V_i - V_c)(.5 - D) + (V_i - .5V_c)D = 0 \tag{19}$$

$$V_c = \frac{V_i}{1-D} \tag{20}$$

Since both the average values of V_{Cr1} and V_{Cr2} are nV_C, the relation between V_i and V_o is obtained as

$$V_0 = n\frac{2V_i}{1-D} \tag{21}$$

From Fig. 4, the interval [t_2, t_3] can be changed by W_r and it is also minimised at $D = D_{min}$. To minimise the conduction loss of D_1, i_{D1} has to reach zero at t_3. From (9), the critical angular resonant frequency W_{rc}, achieving both ZCS and minimum conduction loss of D_1 at $D = D_{min}$, satisfies

$$i_s(t_3) = I_{s,peak} \sin(w_{rc} D_{min} T_s) = 0 \tag{22}$$

From (22), the critical resonant frequency f_{rc} with respect to the switching frequency f_s can be obtained as

$$f_{rc} = \frac{f_s}{2D_{min}} \tag{23}$$

To achieve ZCS of D_1, the resonant frequency has to be higher than f_{rc}. Thus, from (10) and (23), the effective resonant capacitance is designed to satisfy

$$C_r < \frac{1}{w_{rc}^2 L_{lk}} \tag{24}$$

Let us consider the waveform of i_L with respect to its decreasing time and the voltage across the inductor, as showin Fig. 4. During Mode 1, i_L decreases with a slope of $-(V_C - V_i)/L$ and the time of the interval [t_0,t_1] is equal to $(0.5- D)T_s$. Therefore the peak-to-peak value of the boost ripple current ΔI_L is expressed as

$$\Delta I_L = \frac{V_c - V_i}{L}(0.5 - D)T_s \tag{25}$$

From (20) and (21), V_C is $0.5V_o/n$ and V_i is $0.5V_o\,(1 - D)/n$ .Therefore (25) can be rewritten as

$$\Delta I_L = \frac{V_0 D(0.5-D)}{2nLf_s} \tag{26}$$

B. Principle of operation for D >0.5

Figs. 5 and 6 show three topological modes of the converter during a period and their theoretical waveforms, respectively. Prior to Mode 1, i_{p1} flows into S_2 and i_{p2} flows through the body diode of S_3.

Mode 1 [t_0, t_1]: At t_0, S_1 is turned on. The current that had been flowing through D_{S3} flows into S_1 as shown in Fig. 6. Since both S_1 and S_2 are conducting, all voltages across windings of T are zero. Thus, i_L increases linearly as

$$i_L(t) = i_L(t_0) + \frac{V_i(t-t_0)}{L} \quad (27)$$

i_L is equally divided and flows in to S_1 and S_2 .

Mode 2 [t_1, t_2]: At t_1, S_2 is turned off. After a short dead time, S_4 is turned on while its body diode is conducting. As shown in Fig. 6, i_L decreases linearly as

$$i_L(t) = i_L(t_1) - \frac{.5V_c - V_i}{L}(t - t_1) \quad (28)$$

During this mode, the input power is transferred to the secondary side. The state equations are the same as Mode2 in the non-overlapping region. Thus, v_{Cr1} and is are the same with (8) and (9) in the non-overlapping region as

$$v_{Cr1}(t) = \text{nVc} - (\text{nVc} - v_{Cr1}(t_1)) * \cos w_r\,(t - t_1) \quad (29)$$

$$i_S(t) = \frac{\text{nVc} - v_{Cr1}(t_1)}{z_r} \sin w_r\,(t - t_1) \quad (30)$$

$I_{s,\,peak} \sin w_r\,(t\text{-}t_1)$

The relations among the currents of the secondary side are as follows.

$$I_{Cr1}(t) = -\,i_{Cr2}(t) = 0.5\,i_s(t) = i_0(t) \quad (31)$$

Thus, the switch currents are obtained as

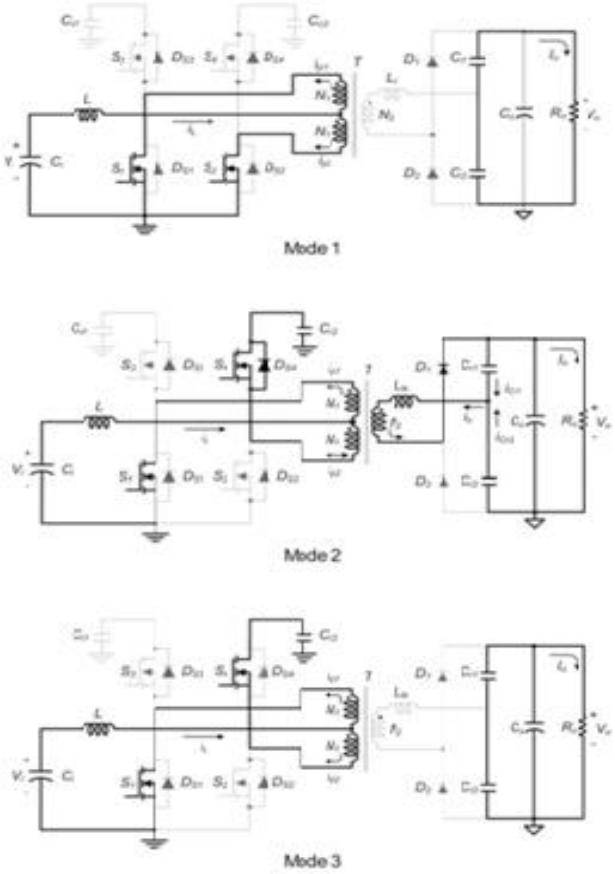


Fig.5 Topological modes and waveforms for D .>0.5

$$i_{s1}(t) = \frac{i_L(t)}{2} + n\,i_s(t) \quad (32)$$

$$i_{s4}(t) = \frac{i_L(t)}{2} + n\,i_s(t) \quad (33)$$

Mode 3 [t_2, t_3]: At t_3, i_{D1} becomes zero and iL decreases as shown in Fig. 6. i_L is equally divided and flows into S_1 and S_4. Since the resonance among C_{r1}, C_{r2} and L_{lk} is terminated, i_{D1} is zero. Therefore the diode D_1 can be turned off softly and the reverse–recovery problem is removed.

Operations of Modes 4, 5, and 6 during the remaining half period are analogous to the operations of Modes 1, 2, and 3,respectively. As in the non-overlapping region, the peak current of io is obtained as

$$I_{s.peak} = \frac{\pi_{w_r} I_0}{w_s} \quad (34)$$

The volt-second balance law of L during the half period provides the relation between V_i and V_C as

$$V_c = \frac{V_i}{1-D} \quad (35)$$

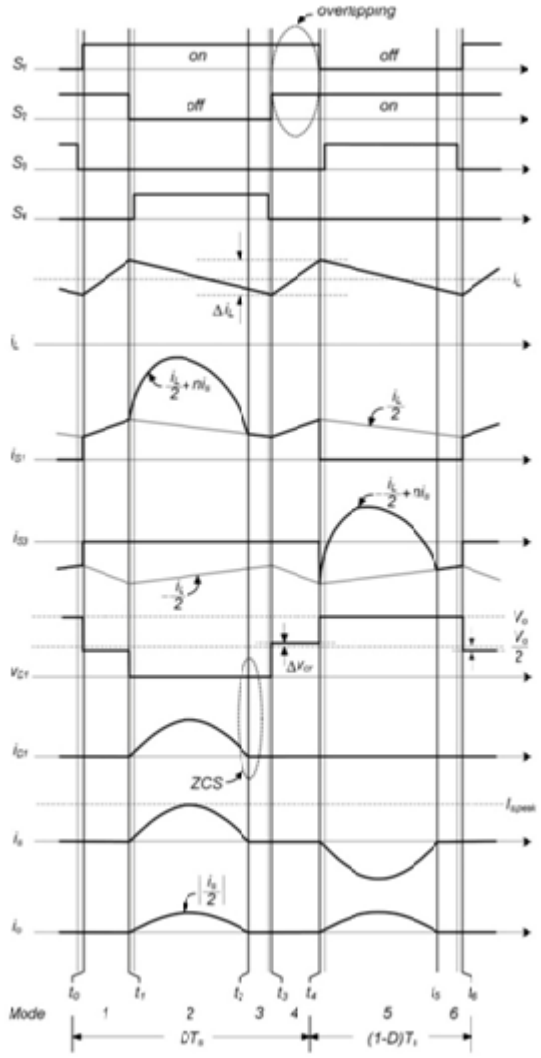


Fig. 6 Theoretical Waveforms of the Proposed Converter for D >.5

Since, from (29), the average values of v_{Cr1} and v_{Cr2} are nV_C, the relation between V_i and V_o is given by

$$V_0 = n\frac{2V_i}{1-D} \quad (36)$$

From (20), (21), (35) and (36), it is recognised that V_C is a constant valueV_o /2n, irrespective of the input voltage. From Fig. 6, the interval $[t_2, t_3]$ can be changed by w_r and it is also minimised at $D = D_{max}$. To minimise the conduction loss of the diode D_1, i_{D1} has to reach zero at t_3. From (30), w_{rc} achieving both ZCS and minimum conduction loss of D_1 at $D = D_{max}$, satisfies

$$i_s(t_3) = I_{s,peak}\ \sin(w_{rc}(1 - D_{\max})T_s) = 0 \quad (37)$$

From (37), f_{rc} can be obtained as

$$f_{rc} = \frac{f_s}{2(1-D_{min})} \quad (38)$$

For ZCS of D_1, C_r is designed to satisfy

$$C_r < \frac{1}{w_{rc}^2 L_{lk}} \quad (39)$$

During Mode 1, i_L increases from t_0 to t_1, hence its increasing time is $(D–0.5)T_s$. Since i_L increases with a slope of V_i /L, the peak-to-peak value of the boost ripple current

$$\Delta I_L = \frac{V_i}{L}(0.5 - D)\,T_s \quad (40)$$

From (36) $V_i = 0.5\frac{V_0(1-D)}{n}$ Therefore (40) can be rewritten as

$$\Delta I_L = \frac{V_0(D-0.5)(1-D)}{2nLf_s} \quad (41)$$

Assuming that V_o is a constant value, Fig. 7a shows the theoretical peak-to-peak values of the boost current which are expressed as (26) and (41) in D<0.5and D>0.5,respectively. Figs. 7b and 7c show theoretical waveforms of the Boost inductor current. All vertical axes are normalised with respect to V_o / (2nfsL). As D approaches 0.5, the magnitude of the ripple current moves in close to zero, as shown in Fig. 7a.Therefore the ripple current of the boost inductor is reduced in comparison to the conventional current-fed push–pull converter in Fig. 1 if the converter is designed to operate in the duty ratio near 0.5. It is also seen that the inductor current varies smoothly throughout the full range of duty ratio. Therefore the inductor current has a smooth transition between D >0.5 and D<0.5, and the converter can operate properly throughout a wider range of input voltage rather than the conventional current-fed push–pull converter.

Flux unbalance is one of the major considerations in the design of push–pull converters. Particularly, in a conventional voltage-fed push–pull converter, unequal volt second product across each half primary, which is usually generated from unequal turns-ratios or unequal duties, causes the flux unbalance problem. Sometimes, a large amount of flux unbalance saturates the core and destroys the switching devices. In case of the voltage-fed push–pull converter, a current-mode control can eliminate the flux unbalance problem by limiting the peak current of main switches [14].However, in the current-fed push–pull converter, implementation of the current-mode control is difficult since each main switch current does not increase monotonously. Therefore its power circuit has to provide the inherent corrective mechanism of the flux unbalance. In the conventional current-fed push–pull converter in Fig. 1,the unbalance correction is provided by the high impedance boost inductor feeding the transformer's centre tap. Since the larger switch current than the load demand causes the voltage drop on transformer's centre tap because of the high-

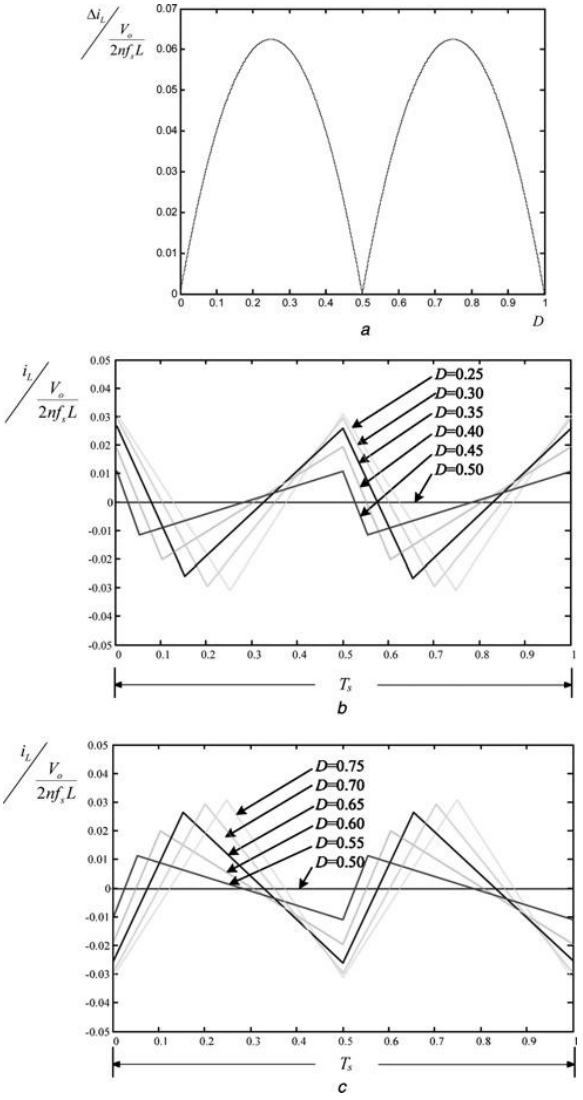


Fig. 7 Inductor ripple current with respect to duty ratio
a. Peak-to-peak value of inductor ripple currents
b. Waveforms of inductor ripple currents for D <0.5
c. Waveforms of inductor ripple currents for D > 0.5

impedance boost inductor, the volt-second product in that half-period is decreased and brings the switch current back down [7]. In the proposed converter in Fig. 2, the flux unbalance is also not a serious problem since the converter provides similar inherent corrective mechanism by employing two clamping capacitors. Although the larger switch current than the load demand is flowing, the high-impedance boost inductor decreases the voltage of relevant clamp capacitor and causes a voltage drop at transformer centre tap. Therefore the volt-second product in that half-period is decreased and brings the MOSFET current back down. If single clamping capacitor configuration as in [9] is employed in the proposed converter, the converter cannot provide aforementioned inherent corrective mechanism.

III. DESIGN PROCEDURE

The switching frequency f_s and the range of input voltage are given, and the output voltage is fixed.

(i) Decide V_C which determines the voltage stress on the primary switches. V_C is usually selected lower than 1.5 times of the maximum input voltage to use low on resistance MOSFETs.
(ii) Obtain the range of D at the given input voltage ranges from (20) to (35).
(iii) Obtain the turns-ratio of T from (20) and (21) as follows:

$$n = \frac{V_0}{2V_c} \qquad (42)$$

(iv) Obtain the critical resonant frequency f_{rc} to meet ZCS conditions (23) and (38), respectively. The higher resonant frequency of two calculated values is selected to provide ZCS of the rectifying diodes throughout the entire range of the input voltage.
(v) Determine the resonant capacitors C_{r1} and C_{r2} from (24) or (39). The capacitors C_{r1} and C_{r2} usually have the same value. L_{lk} is the estimated or measured leakage inductance depending on the winding method and turns-ratio of T.
(vi) Determine L if a maximum ripple current $\Delta I_{L,max}$ is given. From (26) and (41), the following equations are obtained as

$$L \cong \frac{V_0 D(0.5-D)}{2nf_s \Delta I_{L,max}} \quad \text{for } D < 0.5 \qquad (43)$$

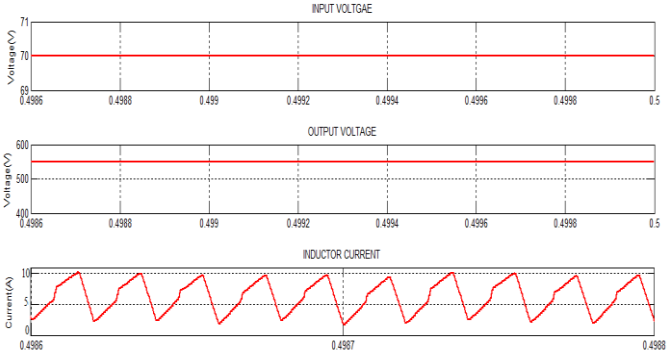
$$L \cong \frac{V_0 (D-0.5)(1-D)}{2nf_s \Delta I_{L,max}} \quad \text{for } D > 0.5 \qquad (44)$$

The largest value of L, calculated in the entire duty range obtained from the design procedure (ii), is selected. From Fig. 5a, the largest value of L is decided at one of the D =0.25, 0.75, D_{min} and D_{max}.

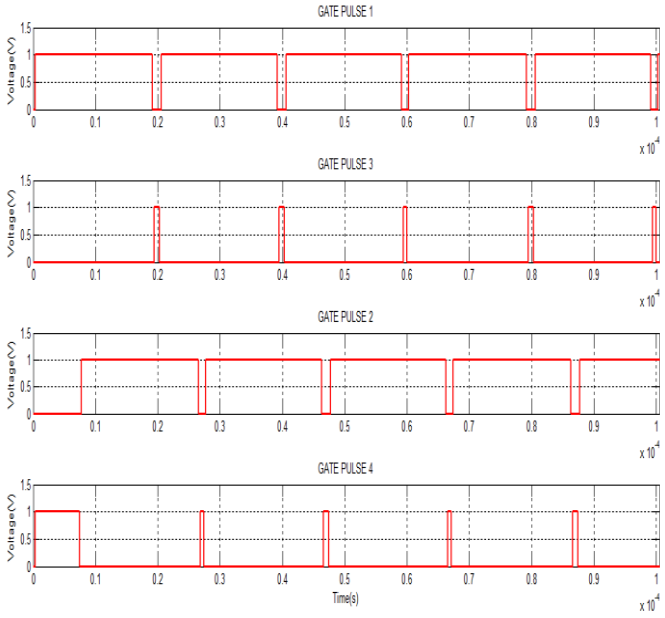
(vii) Peak voltage stress on D1 and D2 is Vo. Selection of the semiconductor devices is a tradeoff of the power conversion efficiency and cost of the converter.

IV. SIMULATION RESULTS

The circuit model of the proposed pushpull converter can be implemented and simulated using Matlab/Simulink both . Figure shows the simulation results of modes. The parameters are chosen as V_i = 70-80V, V_o = 550V, switching frequency Fs = 200 KHz, Po = 550W, capacitors Cr1 = Cr2 = .3µF, inductor L = 2.9µH.



(a)



(b)

Fig.8 Simulation waveforms of the proposed converter

Fig.8 shows the simulation waveforms of the proposed converter. The operation of this converter is verified here. From fig.8 (a), it can be seen that the input voltage is well regulated at 70V and the converter is operated in step-up mode. The waveform of the input inductor current is also shown in Fig.8 (a).The gate pulse of the four switches are shown in Fig.8 (b).

V. CONCLUSION

This paper presents an improved High step-up resonant push- pull converter. The circuit configuration of the proposed converter is very simple and it is modified from the conventional push-pull converter. The proposed converter have wider step-up voltage gain than the conventional push-pull converter. Also, The proposed converter conserves the inherent advantages of the conventional current-fed push–pull converter such as high voltage conversion ratio, low conduction loss of switches and so on. Moreover, the proposed converter employs the voltage-doubler rectifier to alleviate the reverse–recovery loss of the rectifying diodes and to provide much higher voltage conversion ratio. The theoretical analysis and simulation results are provided.

VI. REFERENCES

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