Efficient Power Consumption reduction using Scramble Techniques in Network on Chip

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***Abstract*—an ever more significant fraction of the overall power dissipation of a network-on-chip (NoC) based system on- chip (SoC) is due to the interconnection scheme. In information, as equipment shrinks, the power contributes of NoC links starts to compete with that of NoC routers. In this paper, we propose the use of clock gating in the data encoding techniques as a viable way to reduce both power dissipation and time consumption of NoC links. The projected scramble scheme exploit the wormhole switching techniques. That is, flits are scramble by the network interface (NI) before they are injected in the network and are decoded by the target NI. This makes the scheme transparent to the underlying network since the encoder and decoder logic is integrated in the NI and no modification of the routers structural design is required. We review the projected scramble scheme on a set of representative data streams (both synthetic and extracted from real applications) showing that it is possible to reduce the power contribution of both the self-switching activity and the coupling switching activity in inter-routers links.**

***Keywords*: *Xilinx 12.1,power consumption*.**

I INTRODUCTION

CMOS VLSI is intrinsically a low-power technology. When compared to TTL, ECL or GaAs at similar levels of integration the power dissipated by CMOS is several orders Of magnitude lower[1]. Nowadays, power dissipation is a very burning topic, everybody in search of how to minimize power dissipation in daily use devices like laptops, mobile phones, mp3 players Etc [6]. The dynamic power dissipated by a CMOS circuit is of the form [1]:

$$P_{chip} \propto \sum_{i=1}^{N} C_{load_i} \cdot V_{dd}^2 \cdot f \cdot p_{t_i}$$

Where the sum is complete over all the **N** nodes of the circuit, $\mathbf{C_{load}}$, is the load capacitance at node i, $\mathbf{V_{dd}}$ is the power supply voltage, **f** is the frequency and p_{tt} is the activity factor at node i.

As the number of cores integrated into a system on chip (SoC) increase, the position played by the interconnection system becomes more and more important [2]. Thus, the design of Systems-on-Chip (SoCs) is usually based on the reuse of predesigned and pre-verified intellectual property core that are in interconnected through special communication resources that must handle very tight of performance and area constraints[3].

Sophisticated power-aware, high-level words compilers, active control supervision policies, memory management, bus-encoding techniques, and hardware design tools are demanded to meet these often-conflicting design requirements. This paper focuses on the low power bus-encoding problem [7]. Managing the power of an Integrated Circuit (IC) design has become a major concern of IC designers. In this paper, we focus on techniques aimed at reducing the power dissipated by the network relatives.

In actuality the power degenerate by the network links is as relevant as that dissipated by routers and network interfaces (NIs) and their contribution is expected to increase as technology scales [15].

Most of the previous bus-encoding schemes were designed to minimize transition activities on each signal line as if each line were isolated from neighboring lines, hence ignoring coupling effects. Such an assumption may be valid for off-chip buses where the impedances of transmission lines are appropriately adjusted [8].

A novel intra cache-block spatial locality predictor, to identify words unlikely to be used before the block is evicted. A static packet encoding technique which leverages spatial locality prediction to reduce the network activity factor, and hence dynamic energy, in the NoC routers and links. The static encoding requires no modification to the NoC and minimal additions to the processor caches to achieve significant energy savings with negligible performance overhead. A complementary dynamic packet encoding technique which facilitates additional energy savings in transmitted its, reducing switching activity in NoC links and routers via light-weight micro architectural support [10].

The basic elements which forms a NoC-based interconnect are network interfaces (NIs), routers, and links. As technology shrinks, the power dissipated by the links is as relevant as (or more relevant than) that dissipated by routers and NIs. In this paper we focus on power dissipated by network links. Links dissipate power due to the switching activity (both self and coupling) induced by subsequent data patterns traversing the link [2].

Data compression is an efficient method to decrease power dissipation and by removing the extra redundancy the data can be accurately approximated as a random sequence. Even if compression is not used we believe that a random process is a reasonable approximation for the sequence on a data bus for our purpose [1]. We focus on data encoding schemes as a viable way to reduce power dissipated by the network links. The basic idea is to opportunely encode the data before their injection in the network in such a way as to reduce the switching activity of the links by using the clock gating techniques.

The rest of this brief introduces the scheme by first summarizing data encoding and the related works are considered in Section II. Then, in Section III, the proposed scheme is presented. Section IV and V presents a experimental Results and performance analysis to illustrate the effectiveness of the approach. Finally, the conclusions are summarized in Section VI.

II. RELATED WORK AND DATA ENCODING SCHEMES

The interconnection network dissipates a significant fraction of the total system power budget. For this reason, the design of power efficient interconnection networks is today recognized as a key issue. Several techniques have been proposed in the literature to reduce the power dissipated by the links of a NoC.

In this subsection, we review the sub-set of them which use data encoding schemes as main mechanism to reduce power dissipation [2].

The data encoding schemes we present in this paper have been already introduced by the authors in [15]. In this paper, the proposed schemes are discussed in more details and assessed by means of both a quantitative analysis and an experimental analysis.

The data encoding techniques may be classified into two categories. In the first class, encoding techniques concentrate on lowering the power due to self-switching activity of individual bus lines while ignoring the power dissipation owing to their coupling switching activity. In this category, bus invert (BI) and INC-XOR have been proposed for the case that random data patterns are transmitted via these lines. On the other hand, gray code, functioning-zone encoding, and T0-XOR were suggested for the case of correlated data patterns. Function-specific approaches have also been proposed [15].

The basic idea of the proposed approach is encoding the flits before they are injected into the network with the goal of minimizing the self-switching activity and the coupling switching activity in the links traversed by the flits. In fact, self-switching activity and coupling

switching activity are responsible for link Power dissipation.

The scheme presented in [14] dealt with reducing the pairing switch. In this technique, a complex encoder counts the number of Type I (Table I) transitions with a weighting coefficient of one and the number of Type II transitions with the weighting coefficient of two.

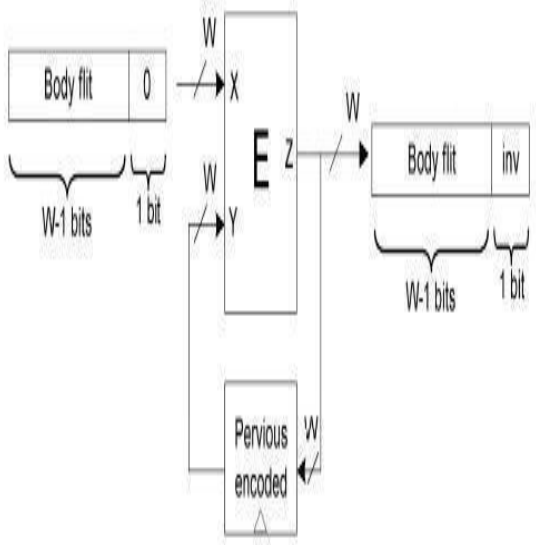

Figure.1 Block diagram of encoding schemes

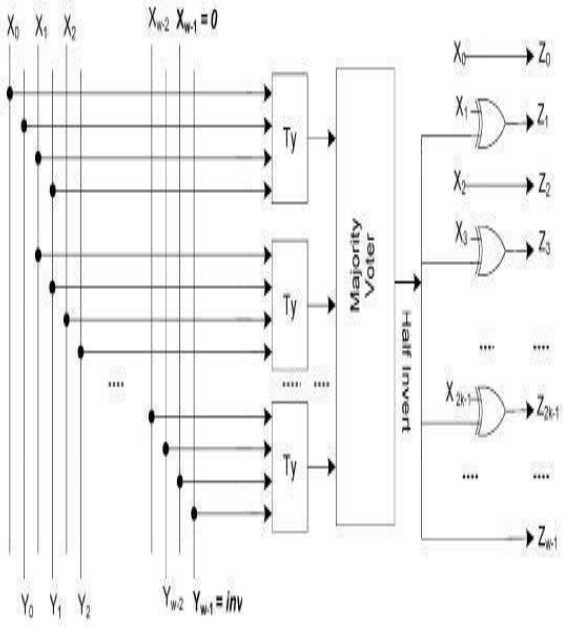

Figure.2 Encoding scheme I

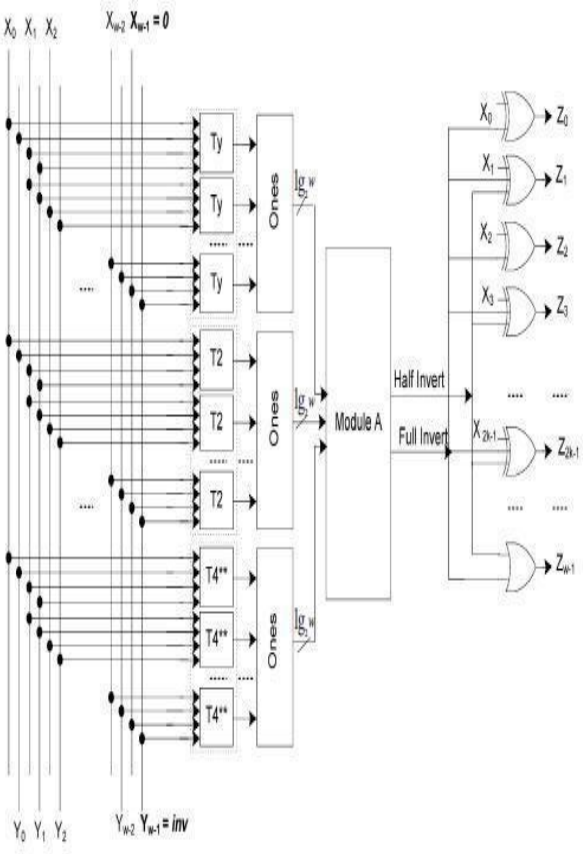

Figure.3 Encoding scheme II

The authors in [15] consider a link width of w bits. The generic block diagram shown in Fig. 1 is the same for all three encoding schemes proposed in this paper and only the block E is different for the schemes. To make the decision, the previously encoded flit is compared with the current flit being transmitted. This latter, whose w bits are the concatenation of w − 1 payload bits and a "0" bit, represents the first input of the encoder, while the previous encoded flit represents the second input of the encoder which is based on the odd invert condition [Fig. 2].

The w − 1 bits of the incoming (previous encoded) body flit are indicated by Xi (Yi), i = 0, 1, . . . ,w − 2.

The w th bit of the previously encoded body flit is indicated by inv which shows if it was inverted (inv = 1) or left as it was (inv = 0). In the encoding logic, each Ty block takes the two adjacent bits of the input flits (e.g., X1X2Y1Y2, X2X3Y2Y3, X3X4Y3Y4, etc.) and sets its output to "1" if any of the transition types of T_y

is detected. This means that the odd inverting for this pair of bits leads to the reduction of the link power dissipation (Table I). The T_y block may be implemented using a simple circuit.

The second stage of the encoder, which is a majority voter block, determines if the condition given in **Ty > (w − 1)/2** is satisfied(a higher number of 1s in the input of the block compared to 0s). If this condition is satisfied, in the last stage, the inversion is performed on odd bits. The decoder circuit simply inverts the received flit when the inversion bit is high.

Similarly in Figure.3, In the proposed encoding scheme II, we make use of both odd (as discussed previously) and full inversion. The full inversion operation converts Type II transitions to Type IV transitions. The scheme compares the current data with the previous one to decide whether the odd, full, or no inversion of the current data can give rise to the link power reduction. where the Types were proposed in [14]. Here 1s blocks which count the number of 1s in their input.

The output of these block has the width of $\log_2 w$. The output of the top 1s block determines the number of transitions that odd inverting of pair bits leads to the link power drop The middle 1s block identifies the number of transitions whose full inverting of pair bits leads to the link power drop to end with the bottom 1s block specifies the number of transitions whose full inverting of pair bits leads to the increased link power. Based on the number of 1s for each conversion type, Module A decides if an odd invert or full invert action should be performed for the power reduction.

The proposed encoding schemes using clock gating are agnostic with respect to the underlying NoC architecture in the sense that their application does not require any modification neither in the routers nor in the links. An extensive evaluation has been carried out to assess the impact of the encoder and decoder sense in the NI. The scramble implement the proposed schemes using clock gating have been assessed in terms of power dissipation and silicon area.

III PROPOSED ENCODING SCHEMES

The general scheme of the proposed approach is depicted in Fig. 4. The basic idea is to apply an encoding technique end-to-end taking advantage of the wormhole switching technique [2]. In this paper, we propose the use of **clock gating techniques** in the data encoding schemes as a viable way to reduce both power dissipation and energy consumption of NoC links.

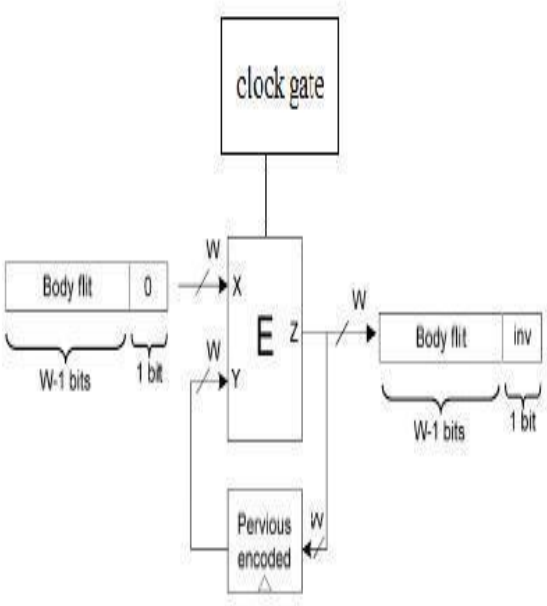

Figure.4 proposed block diagram

CLOCK GATING

Gated clock is a well known method for reducing power consumption in synchronous circuits. By this process the clock signal is not applied to the flip flop when the circuit is in inactive condition. This reduces the power consumption.

In a digital route the power utilization can be accounted due to the following factors:

1) Power devoted by combinatorial circuit whose values are changing on each clock edge 2) Power consumed by flip-flops. From the above two, the second one contributes to most of the power usage.

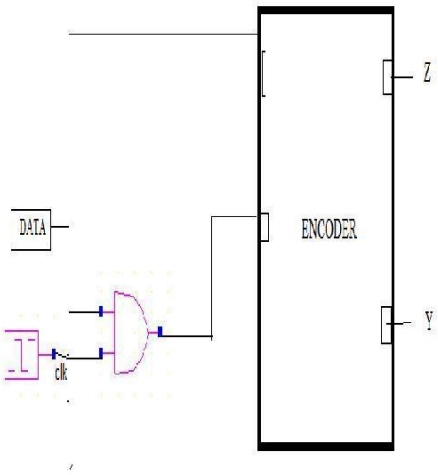

Figure.5 Proposed Clock gating technique

In the beyond two, the second one contribute to most of the power usage.

A flip flop consumes power whenever the applied clock signal changes, owing to the charging and discharging of the capacitor. If the occurrence of the clock is high then the power consumed is also high. Gated clock is a technique to decrease this frequency.

Note the AND operation between load and clk signal. Here the clock to the flip flop "E" is said to be gated. The code point is that, the output has to modify only when load is '1' at the rising border of clock. So it is useless to make the flip flop when the load signal is '0'.If the load signal changes especially infrequently, then the above gated clock code will result in a low power design which is shown in the Fig. 5

IV EXPERIMENTAL RESULTS

The proposed Data encoding schemes with clock gating technique are simulated by using Xilinx ISE 12.1i and implemented in sparten-6 FPGA processor.

V PERFORMANCE ANALYSIS

The performance of the our proposed scheme with existing scheme are analyzed based on the time consumption which was given in Fig. 6.

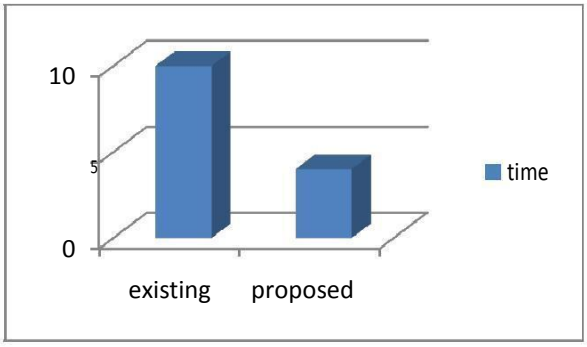

Figure. 6: Time comparison chart of existing and proposed schemes

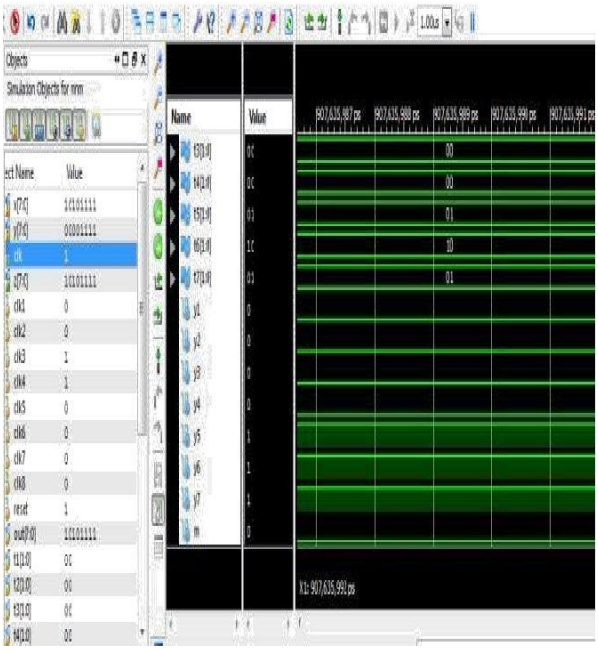

Figure. 7: Simulation Results for data encoding schemes with clock gating

VI CONCLUSION

The power dissipated by the links of a NoC accounts for a significant fraction of the total power budge. In this paper, we have proposed the use of clock gatng in the data encoding techniques as a viable way to reduce both power dissipation and time consumption of NoC links. The proposed schemes are transparent to the underlying NoC infrastructure as they operate on an end-to-end basis.

No modification of the router architecture is needed as well as links width. Only the NI is augmented with the encoding/decoding logic that, although represents an overhead, does not introduce a significant penalty both in terms of cost (i.e., silicon area) and latency. The proposed encoding schemes have been compared with several encoding schemes proposed in literature on a set of representative data streams both synthetic and extracted from real applications.

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