Design and Implementation of Fast and Low Power Locking in DPLL

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Abstract - This paper presents low power and low locking time digital phase locked loop. DPLL is designed and simulated in tanner EDA and by using 0.18um technology. This design is based on current starved voltage controlled oscillator. This design consumes 4.47mW power and takes 0.312us to lock.

Keywords: Phase locked loop, Tanner, Voltage controlled oscillator.

I. INTRODUCTION

A Phase Locked Loop (PLL) is a circuit that synchronizes an oscillator‘s output signal with a reference or input signal in both frequency and phase. The phase error between the oscillator‘s output signal and the reference signal is constant

(not necessarily zero) when the PLL is locked (reference input and oscillator output are synchronized). If a phase error builds up, the feedback control mechanism acts on the oscillator to reduce the phase error to a minimum [1, 5, 10, 14].

PLLs are a well established and very widely used circuit technique in modern electronic systems, which are used primarily in communication systems. In essence, PLLs are circuits in which the phase of a local oscillator is maintained close (or locked) to the phase of an external (reference) signal [3].

The PLL differs from other feedback systems in that it operates on phase deviations rather than signal amplitudes and the variable of interest changes dimension through the loop, shown in Fig 1 (the reference and oscillator signals are used interchangeably with input *x (t)* and output *y (t)*, respectively). The input signal (reference) is usually a phase-modulated periodic signal, for example

$$x(t) = A\cos[\omega_{in}t + \Phi_n(t)] \quad (1)$$

Where ω_{in} is the input angular frequency, *A* is the input signal magnitude, $\Phi n\ (t)$ is the excess phase.

The total phase of this signal is defined as:

$$\Phi_{in}(t) = \omega_{in}t + \Phi_n(t) \text{ and} \quad (2)$$

The instantaneous (angular) frequency as:

$$\Omega_{in}(t) = d\Phi_{in}(t)/dt = \omega in + d\Phi_n(t)/dt \quad (3)$$

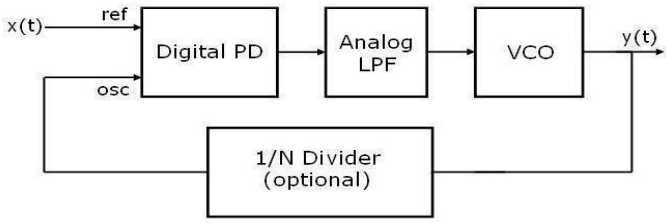

Fig. 1 Block diagram of the digital PLL

The Scope of static and dynamic limits of stability of a PLL is shown below in Figure 2

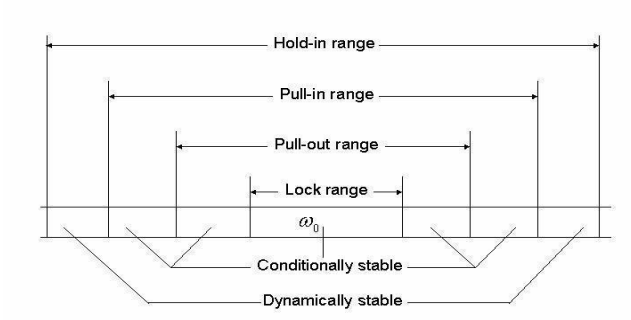

Fig. 2: Scope of static and dynamic limits of stability of a PLL

II. DPLL DESIGN

A Digital PLL (DPLL) consists mainly consists; voltage controlled oscillator, phase frequency detector, charge pump, low pass filter and divider network.

A phase detector is a circuit that detects the difference in phase between its two input signals. It detects the phase difference between the reference frequency and the controlled slave frequency. Some PFD‘s also detect frequency errors; they are then called phase frequency detectors [8, 11 and 16].

Fig.3 is schematic of sequential phase detector design using Tanner S Edit tool. The PFD is build from two D F/Fs whose outputs are denoted Qa (Up) and Qb (Down) with reset features. The inputs to the two clocks are the reference A (f_{ref}) and feedback signals B (f_{fb}). The D inputs are connected to VDD—always remaining high. The outputs are either ―UP‖ or ―DN‖ pulses. These outputs are both connected to an AND gate to the reset of the D-F/Fs.

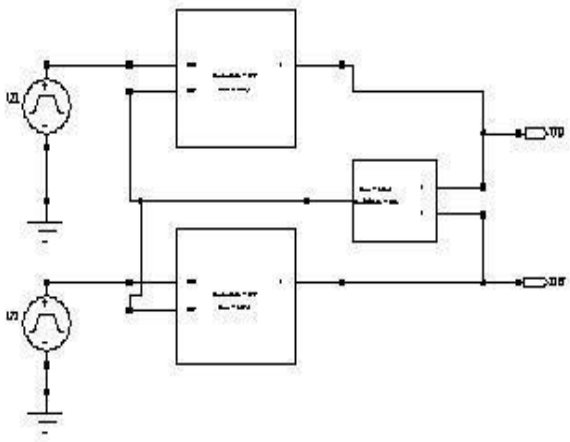

Fig. 3 schematic of sequential phase detector

The Loop filter is the brain of the DPLL. If the loop-filter values are not selected correctly, it may take the loop too long to lock, or once locked small variations in the input data may cause the loop to unlock [2, 10]. Reducing the band-width of the filter also reduces the capture range of DPLL. The phase transfer function of the DPLL

$$H(s) = \Phi clock / \Phi data = Kpd\ Kf\ Kvco / s + \beta.Kpd\ Kf\ Kvco$$

With $s = j\omega$ and the feedback factor is β which is given as

$$\beta = 1/N$$

The transfer function of the loop filter is given by

$$K_f = 1/1+ j\omega RC$$

$$=1/1+sRC$$

The loop filter used with phase detector is simple RC low-pass filter. Since the output of the phase detector is oscillating, the output of the filter will show a ripple as well, even when the loop is locked [10]. So a ripple on the output of the loop filter equal to clock frequency will modulate the control voltage of the VCO. The natural frequency of the resulting second order system is given:

$$W_n = [KpdKvco/N\ (R1+R2)\ C]\ **1/2$$

Kpd=Phase detector gain and
Kvco=VCO gain

Because the input variable of VCO is frequency, it always has a 1/s term in the transfer function to integrate this frequency to phase. Designed filter is shown in Figure 4.

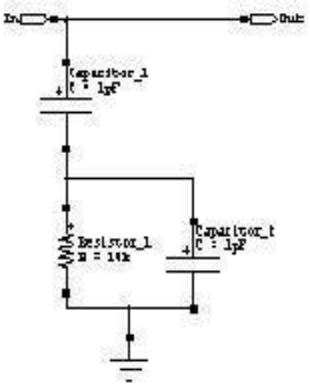

Fig. 4 LPF circuit

The transfer function of the above loop filter is

$$F_1(s) = \frac{1 + s\tau_2}{s\tau_1(1 + s\tau_3)} \quad (11)$$

Where $\tau_1 = R_b(C_1 + C_2)$ (12)

$$\tau_2 = R_1 C_1 \quad (13)$$

$$\tau_3 = \frac{R_1 C_1 C_2}{C_1 + C_2} \quad (14)$$

And R_b is the input impedance of the filter, which is represented by the ratio of the voltage to the current input from the charge pump.

The newly added capacitance, C2, should be about one tenth of the C1. This is a common design practice used when designing the loop filter for a PLL. This circuit results in the following transfer function Z(s):

$$Z(s) = R + \frac{1}{C_1 s}$$

Because C2 is such a small value, it can be ignored for simplicity in the calculations. The loop becomes more stable as R increases.

The charge-pump circuit comprises of two switches that are driven with *UP* and *DN* outputs of PFD. The charge-pump injects the charge into or out of the loop filter capacitor . This average voltage adjusts the frequency of the subsequent oscillator circuit.

The frequency divider is an important building block in today‘s RFIC and microwave circuits because it is an integral part of the phase-locked loop (PLL) circuit. In a typical PLL loop, the output of the voltage-controlled oscillator (VCO) is divided down by the frequency divider. The divided signal is fed into the phase detector for comparison. The output phase difference is used to adjust the VCO output frequency. A frequency divider is an electronic circuit that takes an input signal with a frequency, f_{in}, and generates an output signal with a frequency:

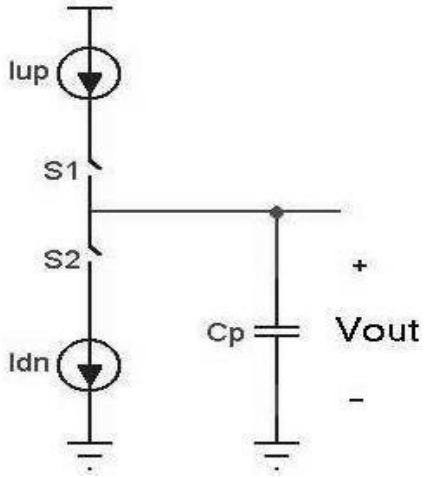

Figure 5: Charge pump

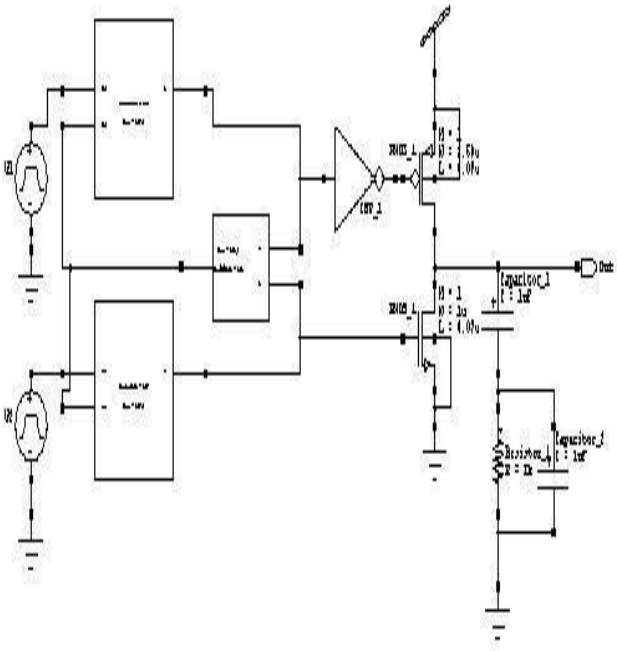

Fig. 6 schematic of Phase Detector with charge pump and loop filter

$f_{out} = \frac{f_{in}}{n}$, where n is an integer.

Asynchronous dividers are the simplest form of frequency dividers. They consist of a series of T flip flops, where each T flip flop is made of D flip flop whose inverted output is connected back to its D input pin, making it a divide by two circuits. The schematic of DFF shown in figure7.

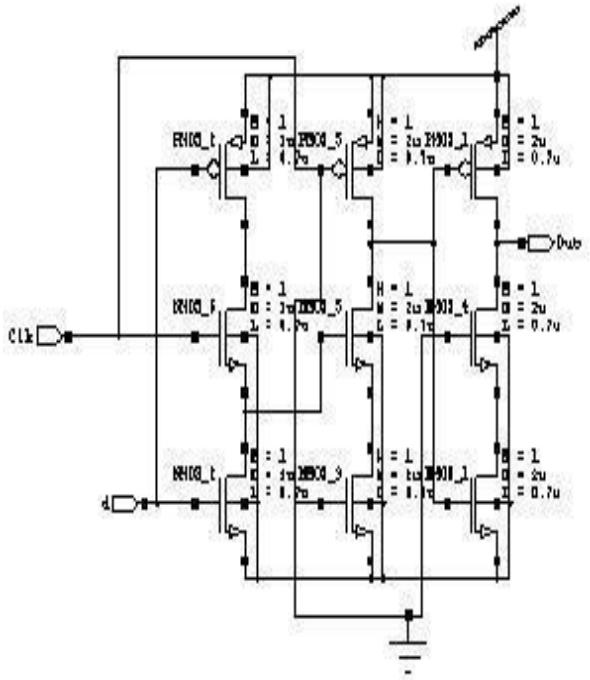

Fig. 7: Schematic of DFF latch

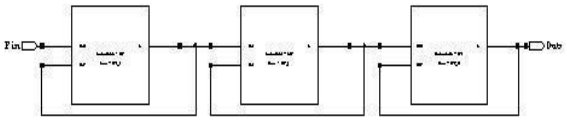

Figure 8: Schematic of Divide by 8

Voltage-controlled oscillator (VCO) ideally generates a periodic signal with a frequency that linearly depends on the input (control) voltage *Vctrl (t).* Grounded input drives the VCO to run at its free-running frequency ωFR. Assuming a linear gain of K_{VCO} (rad/s/V) for this block, which really is not true for practical VCOs, output frequency is found to be:

$$\omega_{out} = \omega_{FRVCO} + K_{ctrl} V \qquad (8)$$

Leading to an output in the form of

$$y(t) = A\cos(\omega_{FR} t + K_{VCO} \int_{-\infty}^{t} V_{ctrl}\, dt) \qquad (9)$$

The excess phase output of the VCO, Φ_{out}, depends not only on the instantaneous value of *Vctrl (t)* but also on its history due to integration of frequency changes in time to form phase information. All these linear time-invariant (LTI) system assumptions on the simple PLL analysis give the following transfer function for the VCO in the s-domain

with a pole at the origin due to integration [1,2,16].

$$\frac{\Phi_{out}}{V_{in}} = \frac{K_{VCO}}{s} \qquad (10)$$

The designing approach used is the current starved approach as the current starved VCO is based on the principle of ring oscillator it has the advantage of wide range of oscillation frequency and smaller size [2, 6, and 15]. The current starved VCO is shown in Figure 9.

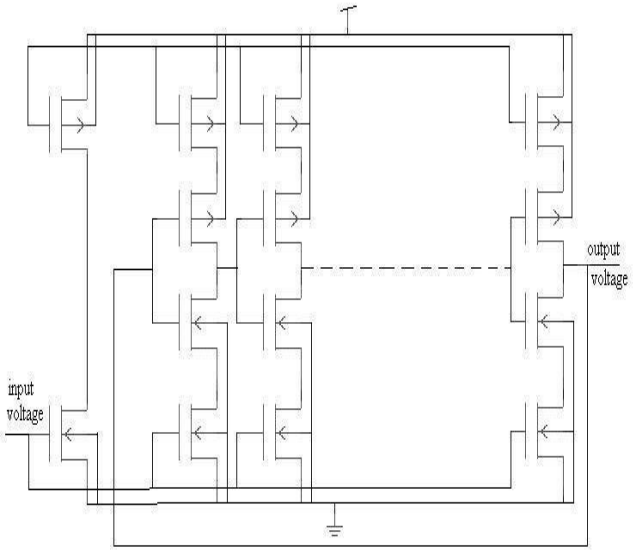

Fig. 9: Current starved VCO

The oscillation frequency is given by

$$F_{osc} = 1/N\,(t_1 + t_2) = I_D/N.\ C_{tot}.V_{dd}$$

Where N=odd number>=5.

Now it is equal to the center frequency

$$f_{center}\ (V_{invco} = V_{dd}/2\ \&\ I_d = I_{dcenter})$$

VCO stops oscillating when $V_{invco} < V_{thn}$,

$$V_{min} = V_{thn}\ \&\ f_{min} = 0.$$

The maximum VCO oscillation frequency f_{max} is determined by finding Id when $V_{invco} = V_{DD}$

The Figure 10 shows the Schematic of DPLL. At first, when the control voltage is not high enough, the VCO doesn‘t oscillate.

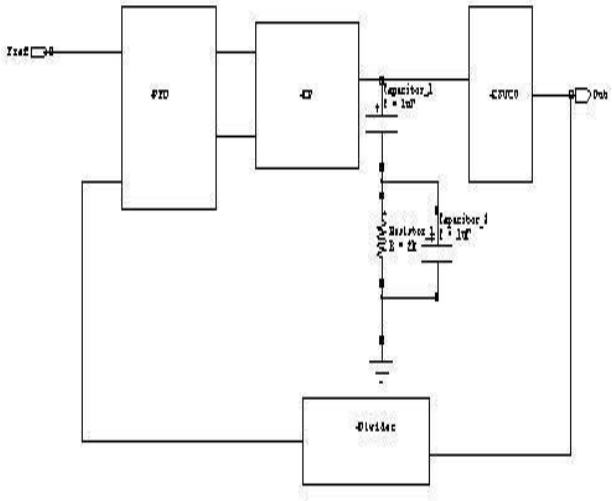

Fig. 10: Schematic design of DPLL

III. SIMULATION/EXPERIMENTAL RESULTS

Phase and Frequency Detector

Figure 6 shows the Schematic of Phase and frequency detector. Two pulse voltage sources are used as the input signals of the Phase and frequency detector.

One is treated as the input of the whole PLL, and the other is treated as the feedback from VCO. The two signals have the same frequency and different phases.

If the rising edge of the_d‘ leads the _dref‘ rising edge, the "Up" output of the phase detector goes high while the"Down" output remains low. This causes the _vco‘ frequency to increase and makes the edges move closer (Figure 4).

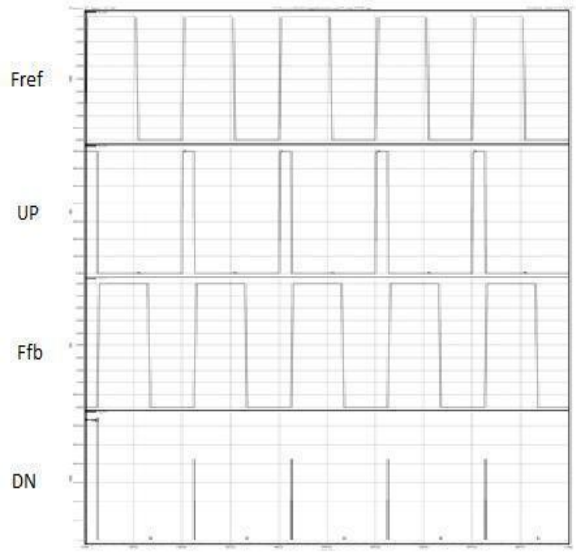

Fig.11: Phase detector output

The transient responses of PFD along with charge pump and loop filter plots is shown in Figure 12.

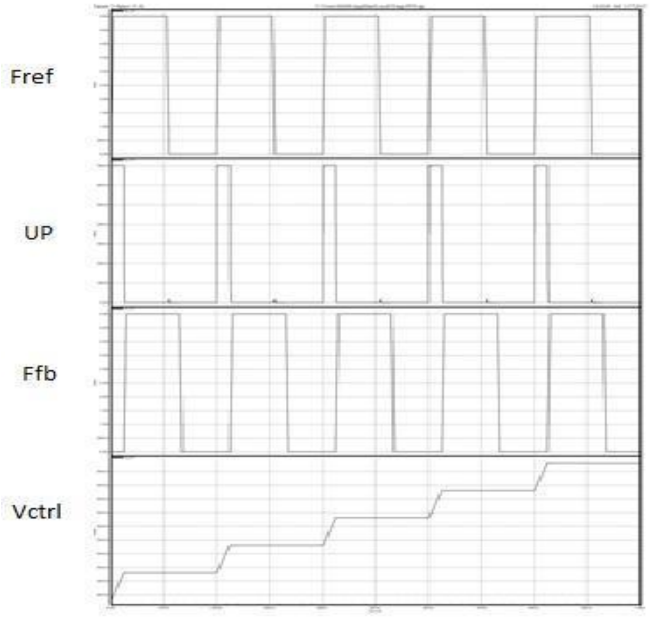

Fig 12: Phase detector with charge pump plots

Loop Filter

The magnitude and phase response plots of the designed filter from HSPICE are shown in Figure 13.

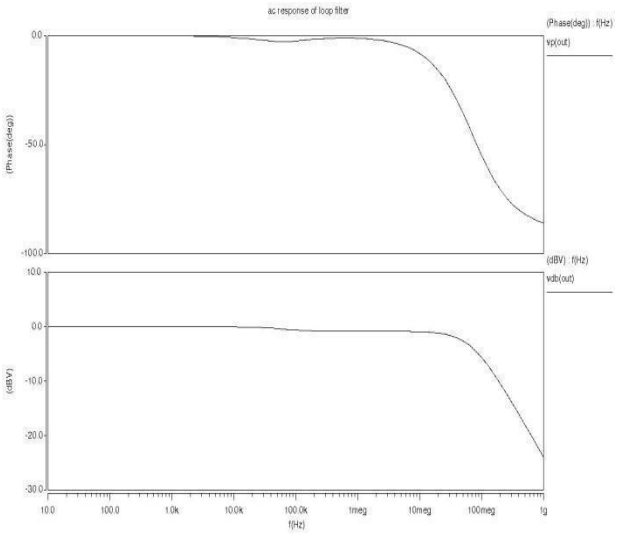

Fig. 13: Magnitude and phase response of loop filter

Voltage Controlled Oscillator

Figure 9 shows the Schematic of current starved VCO. The transient response of current starved VCO is shown below in Figure 14.

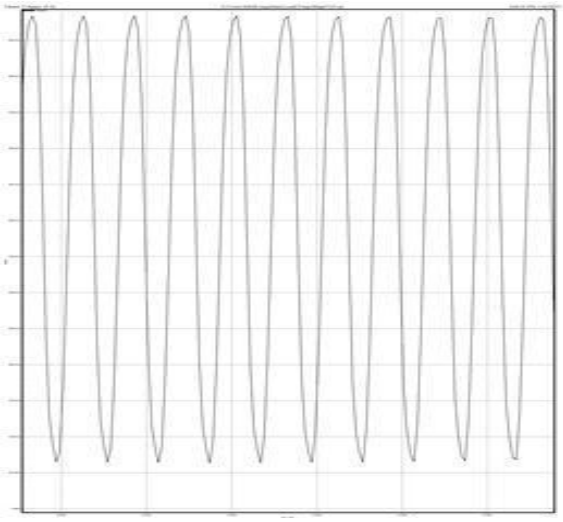

Fig 14: Transient response of current starved VCO

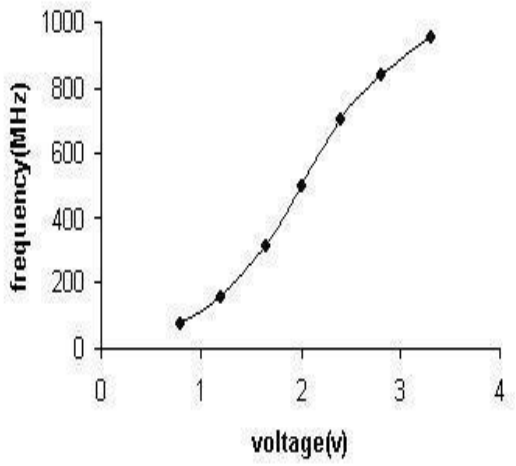

Fig. 15: frequency vs. voltage plot of current starved VCO

Frequency Divider

The transient response of the divide by 8 is shown in Figure16

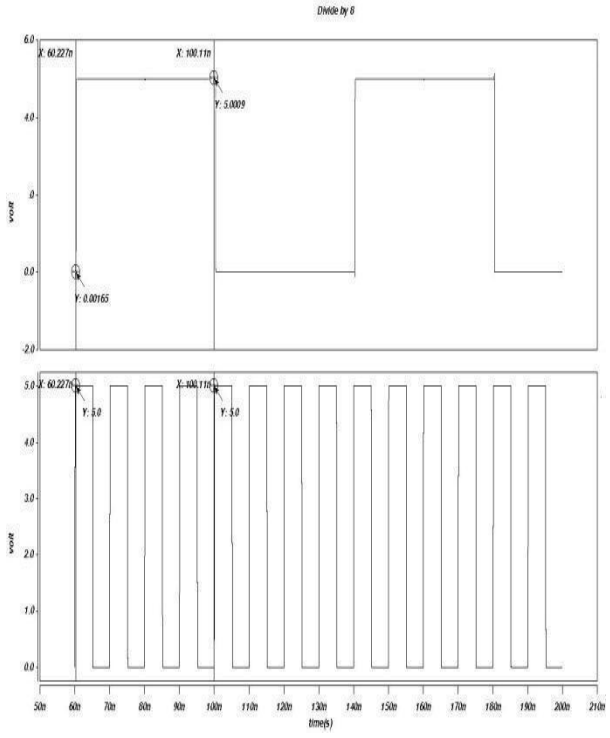

Fig. 16: Transient response of the divide by 8

Digital Phase Locked Loop (DPLL)

Figure shows the Schematic of DPLL. The transient response of the DPLL is shown in Figure17.

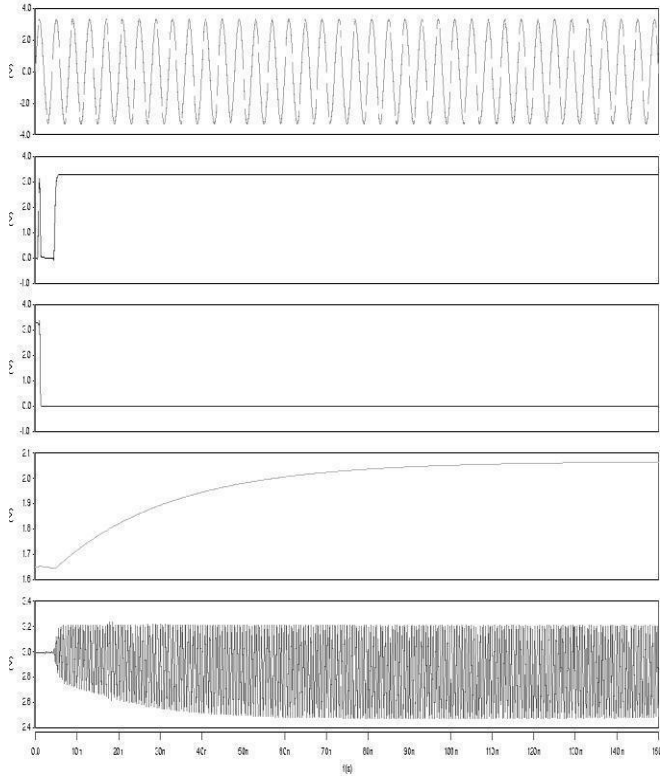

Fig. 17: Transient response of the DPLL

IV. CONCLUSION

A low power and fast locking digital phase locked loop has being designed and simulated. From the simulation results, it was revealed the power consumption of DPLL is 4.47mwatts as compared to 5.14 mW of the DPLL reported by [20].

The simulation results also revealed that lock time of this DPLL is 0.312us which is almost improved by a factor of 3.3 compared to work proposed by [5]. The other important results are summarized in table 1 given below:

Table 1: Digital Phase Locked Loop measured results

Parameters	**Measured Results**
Technology	0.18 micron.
Vdd	1.8V
Power drawn by PFD	7.07nWatts
Gain (up and down)	-35dB
Phase angle	$-\pi$ to $+\pi$
Operating frequency range of VCO	320MHz
VCO Gain (K_{VCO})	263.63radians/s. V
Tuning range of VCO	81-950MHz
Power consumed in VCO	5.809uWatts
Reference frequency of DPLL	40MHz
Lock time	0.312us
Power consumed by DPLL	4.47mWatts

REFERENCES

[1] Behzad Razavi. ―Design of Analog CMOS Integrated Circuits.‖ McGraw-Hall.

[2] H.W. Li R.J. Baker and D.E. Boyce.CMOS Circuit Design, Layout, and Simulation. *IEEE Press*, New York, NY, 1998.

[3]Virendra K. Verma, D. K. Mishra, R. S. Gamad, ―A comparative analysis of frequency synthesizers‖ International journal of Electronics and Communication Engineering ISSN:2278-9901: vol-2, Issue-4,Sep-2013,95-104.

[4]Yue-Fang Kuo, Ro-Min Weng, and Chuan-Yu Liu, ―A Fast Locking PLL With Phase Error Detector‖, *IEEE International Conference*, pp. 423-426, 2005.

[5]Robin R.-B. Sheen, Oscal T.-C. Chen, Robert C.-H. Chang, ―A 1.3V 1.04GHz - 130GHz CMOS Phase-Locked LOOP, *IEEE International Conference*, pp. 569-572, 1997.

[6] Mahmoud Fawzy Wagdy, ―A FAST-LOCKING DIGITAL PHASE-LOCKED LOOP‖, *Proceedings of the Third International Conference on Information Technology: New Generations (ITNG'06)*

[7] Shilpa Ambarish, ―A WIDE-BAND DIGITAL PHASE-LOCKED LOOP,‖ *IEEE International Conference, 2006*.

8] Hwang-Cherng Chow and N.-L. Yeh, ―A New Phase-Locked Loop with High Speed Phase Frequency Detector‖, *IEEE International Conference*, pp. 1342-1345.

[9] Won - Hyo Lee, Jun - Dong Cho and Sung - Dae Lee, ―A High Speed and Low Power Phase-Frequency Detector and Charge – pump, *IEEE International Conference*, pp. 269-272, 1999.

10] Bosco Leung. VLSI for wireless communication.
Pearson education, 2004.

[11] Hwang-Cherng Chow and Nan-Liang Yeh, ―A Lock-in Enhanced Phase-Locked Loop with High Speed Phase Frequency Detector‖, *Proceedings of 2005 International Symposium on Intelligent Signal Processing and Communication Systems*,pp.410-404, Dec2005.

[12] P. Larsson, **"**A 2-1600-MHz CMOS clock recovery PLL with low-Vdd capability,‖ in *IEEE Journal of Solid-State Circuits*, Vol. 34, No.12, pp. 1951-1960, Dec. 1999.

[13] W. Rhee, ―Design of high-performance CMOS charge pumps in phase-locked loops,‖ in *IEEE International Symposium on Circuits and Systems*, pp. 545-548.

[14] F. Gardner. *Phase lock Techniques*. John Wiley & Sons, 1979.

[15] M. S. Lee, T. S. Cheung, and Woo-Young Choi, ―A novel charge pump PLL with reduced jitter characteristics,‖ in *International Conference on VLSI and CAD*, pp.596-598, 1999.

[16] Asad A. Abidi, ―Phase Noise and Jitter in CMOS Ring Oscillators, *IEEE JOURNAL OF SOLID-STATE CIRCUITS*, VOL. 41, NO. 8, AUGUST 2006.

[17] Yun Cheol Han and Kwang Sub Yoon, ―Design of a 3.3V high frequency CMOS VCO with an arithmetic functionality‖, *IEEE International Conference*, pp. 324-327, 2001.

[18]D. Ham and A. Hajimiri, ―Concepts and methods in optimization of integrated LC VCOs,‖ *IEEE Journal of Solid-State Circuits*, vol. 36, no. 6, pp. 896–909, June 2001.

[19] Chih-Ming Hung and Kenneth K. O, ―A Fully Integrated 1.5-V 5.5-GHz CMOS Phase-Locked Loop‖, *IEEE JOURNAL OF SOLID-STATE CIRCUITS*, VOL. 37, NO. 4, APRIL 2002.

[20] Jieh-Tsorng Wu, Mu-Jung Chen, and Cheng-Chung Hsu, ―A *2* V 900 MHz CMOS Phase-Locked LOOP, 1998 *Symposium on VLSI Circuits Digest of Technical Papers.*

[21] Gauri Shankar Singh, Devesh Singh and S.Moorthi, ―Low Power Low Jitter Phase Locked Loop for High Speed Clock Generation‖, Asia Pacific Conference on Postgraduate Research in Microelectronics & Electronics (PRIMEASIA), December 2012.

[22]Arpan Jadhav, Virendra K. Verma ―A Low power CMOS LC VCO in 70nm for RF Applications‖, International journal of Electronics and Communication Engineering ISSN:2278-991X: vol-2, Issue-5,Nov-2013, 179-186,Impact Factor(JCC)(2013): 2.5893

[23]Vikalp Thakur and Virendra K. Verma ―Low Power Consumption Differential Ring Oscillator" International Journal of Electronics and Communication Engineering, pp. 81-92 VOL: ISSN 0974-2166 Volume 6, year 2013.

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