

# Design and Development of a 66.46W Multi-output Soft Switching Active Clamp Fly-back Converter Power Supply

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**Abstract**— This paper describes design and development of a 66.46W multiple output soft switching power supply by using an active clamp fly-back converter switching at 100 KHz. This converter generates the six output voltages required for the power supply from a single input of 270 DC voltage. The presence of the active clamp with fly-back circuit recycles the energy stored in the leakage inductance to reduce the voltage stress at the switch. The active clamped circuit can also help the main switch to turn on at ZVS (Zero Voltage Switching) using the switch output capacitor and transformer leakage inductance. ZVS also limits the turnoff di/dt of the output rectifier, reducing rectifier switching losses and switching noise due to diode reverse recovery.

**Keywords**—Multi output Active Clamp Fly-back Converter, Continuous Conduction Mode (CCM), Zero Voltage Switching (ZVS), Direct Current (DC)

## I. INTRODUCTION

Power supply is nothing but, the power electronic converter circuit which in the system converts electrical energy from one level to another level using semiconductor based electronic switches. In many respects it is the mother of system. It gives the system life by providing constituent and repeatable power to its circuits. If the power supply experiences a failure within itself, it must fail gracefully and not allow the failure to reach the system. The goal of the power supply section is to distribute power effectively to each section of the entire product and to do it in a fashion that meets the needs of each subsection within the product. So as to design a power supply the designers needs to select the technology of each power supply within the system[1].The important issues that influence the stage of design are cost, weight, space, how much heat can be generated within the product, the input power source, the noise tolerance of the load circuits, battery life (if the product is to be portable), and the number of output voltages required and the time to market of the product. According to the comparison table I PWM switching power supplies can be relatively high efficient and the operation is easy to understand. Unlike linear regulators which operate the power transistor in the linear mode, the PWM switching power supply operates the power transistor in both the saturated and cut off states. In these states, the volt-ampere product across the power transistor is always kept low. This EI product within the power device is the loss within all the power semiconductors. So industrially PWM technology is commonly used.

TABLE I. COMPARISON OF FOUR POWER SUPPLY TECHNOLOGIES.

Features	Linear regulator	PWM switching regulator	Resonant Transition switching regulator	quasi resonant switching regulator
Cost	low	High	high	highest
Mass	high	low to medium	low to medium	low to medium
RF noise	none	High	medium	medium
Multiple outputs	no	yes	yes	Yes
Development to production	1 week - months	8 person-months 5persons-months	10person-months 8persons-months	10 person 10persons-months
Efficiency	35-50%	70-85%	78-92%	78-92%

### A. PWM - Switching Topologies

The term topology refers to the arrangement of power components within the switching power supply design. This arrangement has the large bearing on which environment the supply can operate in safely and how much power the power supply can provide to the loads[2].This is the point in the design process where the major costs versus performance tradeoffs are made. A summary of the relative merits of the various topologies is given in table II.

### B. Fly-back Topology

The fly-back topology is the favorite for below 100 – 150W because of its low parts count (hence low cost)and intrinsically better efficiency operating with continuous conduction mode. There are a few differences between forward and fly-back are given in table III given below. The fly-back topology has long been attractive because of its relative simplicity when compared with other topologies used in low power applications[3].The “fly-back transformer” serves the dual purposes of providing energy storage as well as converter isolation, theoretically minimizing the magnetic component count when compared with, for example, the forward converter. A drawback to the use of the fly-back is the relatively high voltage and stress suffered by its switching components. High peak and RMS current stress is a particular problem for fly-backs.

TABLE II. COMPARISON OF THE PWM SWITCHING REGULATOR TOPOLOGIES.

Topology	Power range(w)	Vin dc range	Input isolation	Typical efficiency	Relative parts /cost
Buck	0-1000	5-1000	no	78	1.0

<b>Boost</b>	0-150	5-600	no	80	1.0
<b>Buck-boost</b>	0-150	5-600	no	80	1.0
<b>Forward</b>	0-150	5-600	yes	78	1.4
<b>Fly-back</b>	0-150	5-500	yes	80	1.2
<b>Push pull</b>	100-1000	50-1000	yes	75	2.0
<b>Half bridge</b>	100-500	50-1000	yes	75	2.2
<b>Full bridge</b>	400-2000	50-1000	yes	73	2.5

TABLE III. ADVANTAGES OF FLYBACK TOPOLOGY OVER FORWARD TOPOLOGY

Parameter	Forward	Fly-back
No. of components required	1 Q,T/F,2D,1L,1C	1Q,T/F,1D,1C
Output filter inductor	required	not required
Cost and size	more	significant saving cost and space
Core reset	required	not required

## II. PROPOSED ACTIVE CLAMP FLYBACK TOPOLOGY

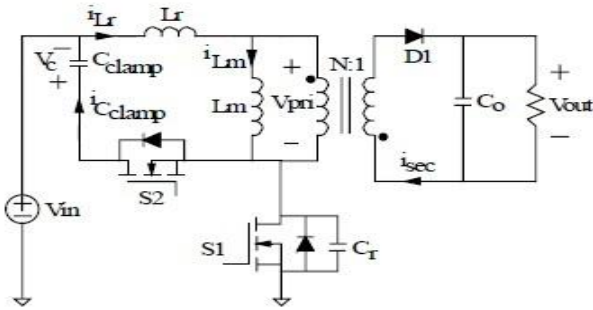


Fig. 1. Simplified schematic of Active Clamp Fly-back Converter

The incorporation of an active clamp circuit into the basic Fly-back topology is shown in Fig.2 In the figure, the fly-back transformer has been replaced with an equivalent circuit model showing the magnetizing and leakage inductances ( $L_r$  represents the total transformer leakage inductance reflected to the primary in addition to any external inductance). Switches  $S_1$  and  $S_2$  are shown with their associated body diodes.  $C_r$  represents the parallel combination of the parasitic capacitance of the two switches. It is this device capacitance resonating with  $L_r$  that enables ZVS for  $S_1$ . With the active clamp circuit, the transistor turn-off voltage spike is clamped, the transformer leakage energy is recycled, and zero-voltage-switching (ZVS) for both primary ( $S_1$ ) and auxiliary ( $S_2$ ) switches becomes a possibility. These advantages come at the expense of additional power stage components and increased control circuit complexity (two switches as opposed to the usual one switch). Figure 3 illustrates the topological states

and Figure 4 the key waveforms for the active clamp fly-back converter. [13] For this description of circuit operation (and for the subsequent development of a design procedure in the next section), the following assumptions are made: Ideal switching components. The magnetizing current is always non-zero and positive (positive direction as defined by Fig.1  $L_r$  (includes the transformer leakage inductance) is much less than the transformer magnetizing inductance,  $L_m$  (typically 5% to 10% of  $L_m$ ); sufficient energy is stored in  $L_r$  to completely discharge  $C_r$  turn on  $S_1$ 's body diode;

$$\pi\sqrt{L_r C_{clamp}} \gg T_{off}$$

Last assumption simply states that one-half the resonant period formed by  $L_r$  and  $C_{clamp}$  is much longer than the maximum off time of  $S_1$ .

$t_0 - t_1$ :

At  $t_0$ , switch  $S_1$  is on, and the auxiliary switch,  $S_2$ , is off. The output rectifier,  $D_1$ , is reversed biased as is the anti-parallel diode of  $S_2$ . The magnetizing inductance (along with the resonant inductance) is being linearly charged just as it would be during the inductor-charging phase in normal fly-back operation.

$t_1 - t_2$ :

$S_1$  is turned off at  $t_1$ .  $C_r$  is charged by the magnetizing current (which is also equal to the current through the resonant inductor).  $C_r$  is actually charged in a resonant manner, but the charge time is very brief, leading to an approximately linear charging characteristic.

$t_2 - t_3$ :

At  $t_2$ ,  $C_r$  is charged ( $V_{DS} = V_{in} + V_c$ ) to the point where the anti-parallel diode of  $S_2$  starts to conduct. The clamp capacitor fixes the voltage across  $L_r$  and the transformer magnetizing inductance to  $V_c$  (at  $NV_o$ ), forming a voltage divider between the two inductances. Since  $C_{clamp}$  is much larger than  $C_r$ , nearly all of the magnetizing current is diverted through the diode to charge the clamp capacitor. Consequently, the voltage appearing across the magnetizing inductance,  $V_{pri}$ , decreases as  $V_c$  increases, according to the voltage divider action described by Eq. (1):

$$V_{pri} = -V_c \frac{L_m}{L_m + L_r} \quad (1)$$

$t_3 - t_4$ :

At  $t_3$ ,  $V_{pri}$  has decreased to the point where the secondary transformer voltage is sufficient to forward bias  $D_1$ . The transformer primary voltage is then clamped by the (very large) output capacitance to approximately  $NV_o$ .  $L_r$  and  $C_{clamp}$  begin to resonate. In order for  $S_2$  to achieve ZVS, the device should be turned on before  $i_{C_{clamp}}$  reverses direction.

$t_4 - t_5$ :

The auxiliary switch,  $S_2$ , is turned off at  $t_4$ , effectively removing  $C_{clamp}$  from the circuit. A new resonant network is formed between the resonant inductor and the MOSFET parasitic capacitances. The transformer primary voltage remains clamped at  $NV_o$  as  $C_r$  is discharged.

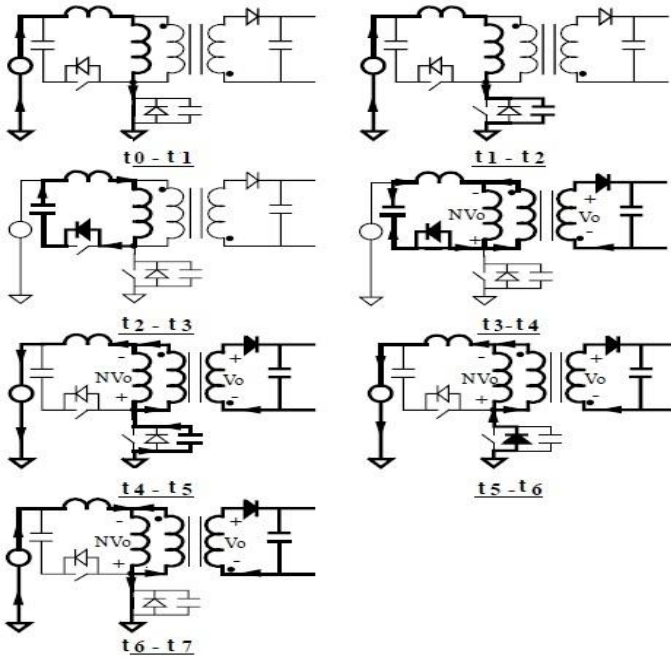


Fig. 3. Active Clamp flyback Topological states.

t5 - t6:

Assuming the energy stored in  $L_r$  is greater than the energy stored in  $C_r$ , at  $t_5$   $C_r$  will be sufficiently discharged to allow  $S_1$ 's body diode to start conducting. The voltage across the resonant inductor becomes clamped at  $V_{in} + NV_o$ . This also fixes the rate of decay of the output rectifier current to:

$$\left. \frac{di(DI)}{dt} \right| = -N \left( \frac{NV_o}{L_m} + \frac{V_{in} + NV_o}{L_r} \right) \quad (2)$$

For  $L_m \gg L_r$  Eq. (2) simplifies to:

$$\left. \frac{di(DI)}{dt} \right| = -N \left( \frac{V_{in} + NV_o}{L_r} \right) \quad (3)$$

It is during this interval that switch  $S_1$  can be turned on under zero-voltage conditions.

t6 - t7:

$S_1$  is on, and the secondary current is decreasing as the resonant inductor current increases. At  $t_7$ , the secondary current decreases to zero (because the resonant inductor current has equalled the magnetizing current), and  $D_1$  reverse biases, allowing the polarity to reverse on the transformer primary. The magnetizing and resonant inductances begin to linearly charge again, starting another switching cycle ( $t_7 = t_0$ ). Note that the length of the time intervals  $t_1$  to  $t_3$  and  $t_4$  to  $t_7$  have been greatly exaggerated in Fig.3 in order to more clearly show the transition periods.

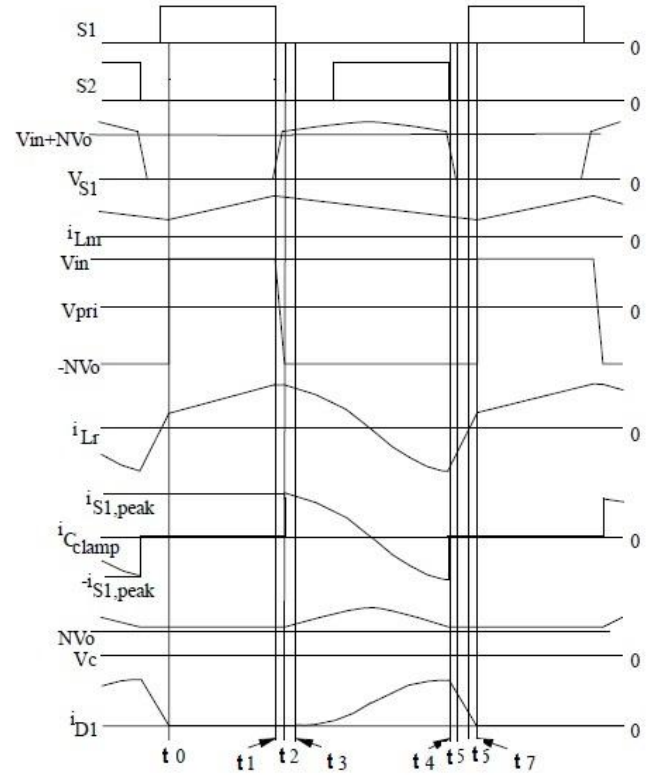


Fig. 4. Active Fly-back steady state waveforms

### III. DESIGN STEPS

STEP 1: Turns ratio (n): The turns ratio  $n$  between transformer primary side to secondary side is given by

$$n = \frac{N_1}{N_2} = \frac{V_{in,min} D_{max}}{V_o (1 - D_{max})}$$

( $D_{max} = 0.55$ , Assumption)  $N_1$  = Primary no of turns  $N_2$  = Secondary no of turns  $V_{in,min}$  = Minimum input voltage  $V_o$  = Output voltage.

STEP 2: Voltage stress of main switch: The voltage stress of main switch is

$$V_{S_{main,max}} = V_{in,max} + nV_o$$

$V_{in,max}$  = Maximum input voltage,  $n$  = Turns ratio

STEP 3: Magnetizing inductance:

$$L_m = \frac{\eta [V_{in} D T_s]^2}{2 P_o (min) T_s}$$

$\eta$  = Efficiency (80%)  $V_{in}$  = Input voltage in volts  $T_s$  = Switching period  $P_o(min)$  = Minimum output power.

STEP 4: Peak current of main switch  $I_{S_{main,peak}}$ : The peak current of main switch,

$$I_{S_{main,peak}} = \frac{P_o}{\eta \cdot V_{in,min} \cdot D_{max}} + \frac{V_{in,min}}{L_m} D_{max} T_{sw}$$

STEP 5: Voltage stress of rectifier diode: The voltage stress of rectifier diode at the transformer secondary side is

$$V_{Do,max} = \frac{V_{inmax}}{n} + V_o$$

STEP 6: Peak secondary diode current: The peak secondary diode current is expressed as

$$I_{Do,peak} = \frac{2P_o}{V_o \cdot (1 - D_{max})}$$

STEP 7: Output filter capacitance Co: The output filter capacitance Co is expressed as

$$C_o = \frac{D_{max} P_o}{f_{sw} V_o \Delta V_o}$$

STEP 8: Calculation of resonant inductance Lr:

Resonant capacitance: Cr = parallel combination of the parasitic capacitance of main switch Smain and auxiliary switch Saux Resonant inductance: Lr = Sum of transformer leakage inductance and external inductance .

Lr is given by:

$$L_r = \frac{1}{4\pi^2 f_r^2 C_r}$$

fr = Resonant frequency Cr = Resonant capacitance Lr = Resonant inductance

STEP 9: Clamp capacitance Cclamp: Clamp capacitance is given by,

$$C_{clamp} = \frac{[(1 - D_{min} V_{in}) T_{sw}]^2}{\pi^2 L_r}$$

D(minV in)=Duty minimum ,Lr=Resonant inductance

STEP 10: Calculation of primary turns Np :

$$N_p = \sqrt{\frac{L_m}{A_L}}$$

STEP 11: Supply Transformer

The core selected for power supply is UU 49/36/28 core. Here primary of the transformer wound on one limb of the U and secondary's are wound on the other limb of the core.

STEP 12: Calculation of secondary turns Ns and inductance LS

Secondary number of turns

$$N_s = \frac{N_p}{n}$$

Secondary inductance

$$L_s = A_L N_s^2$$

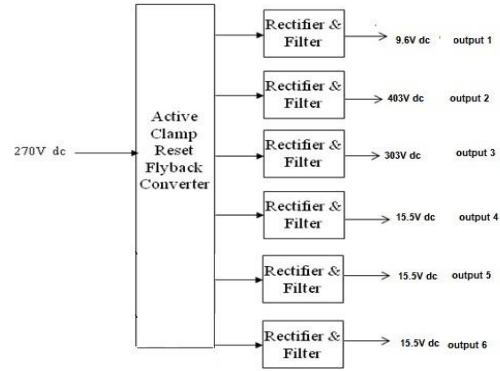
#### IV. EXPERIMENTAL RESULTS

Specifications:

Input: Input Voltage Vin (dc) = 270V ± 1% Switching Frequency=100 KHz

Outputs: Output 1 : 9.6 V, 3.5 A, Output 2 : 15.5 V, 250 mA  
Output 3 : 15.5 V, 250 mA, Output 4 : 15.5 V, 250 mA,  
Output 5 : 403V, 30mA, Output 6 : 303 V, 30mA

##### A. PSpice Simulation Results



Block diagram of the proposed power supply

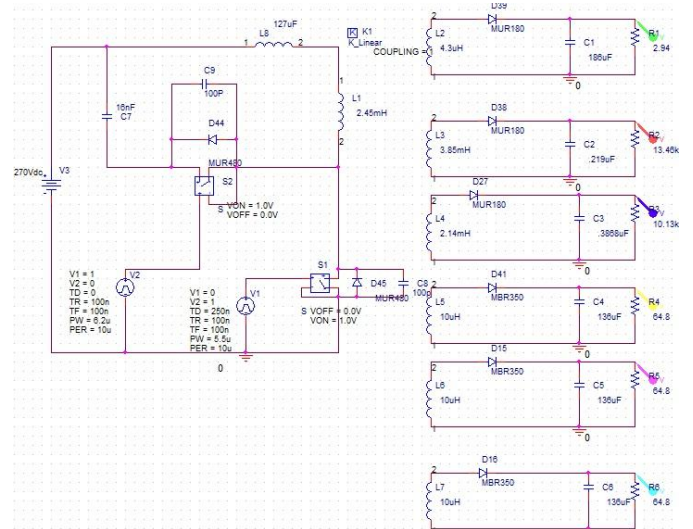


Fig. 7. Active clamp fly-back Converter Primary and secondary circuit.

The above shown in Fig.7 is simulation circuit for the input part of the active clamp fly-back converter. In this technique two switches (S1, S2), parallel to the switches body diodes (D1, D2) and parasitic capacitances (C2, C16) are connected. These two switches are excited by pulse voltage sources V2, V3 shown in Fig. 7 L1 is the magnetizing inductance, L2 is external series resonant inductor, C1 is the clamp capacitor and L4, C4 are the DC input filter for incoming 270 V input. After simulating this circuit the results are captured and shown in below figures. Fig.8 gives the drain to source voltage with respect to the gate voltage. Fig.9 gives drain voltage and drain current, fig.7 shows the primary and secondary part of the active clamp flyback converter and fig.10 gives the output voltages of the active clamp flyback converter. The fig.8 shows the ZVS characteristics of this converter.



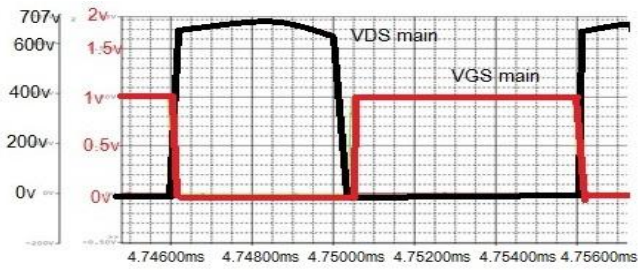


Fig. 8. Drain Voltage (Black) with respect to Gate (Red) Voltage of Main Switch

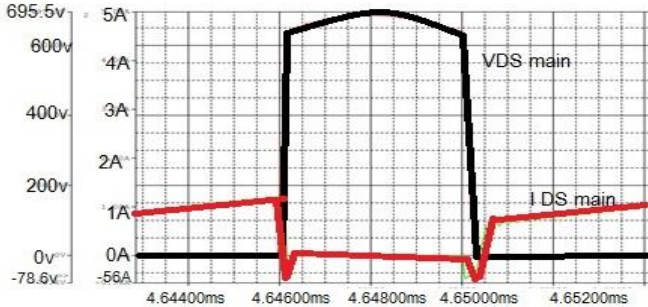


Fig. 9. Drain Voltage (Black) and Drain Current (Red) of Main Switch

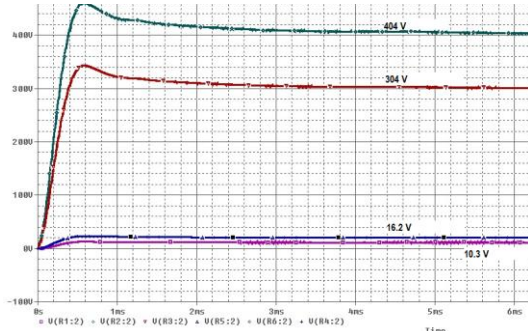


Fig. 10. Output Voltages of the power supply

## B. Hardware Setup and Results

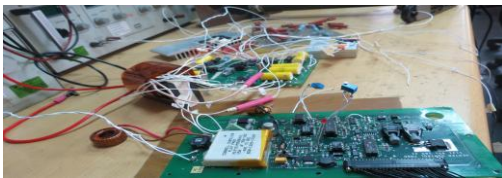


Fig. 11. Hardware Setup of Active Clamp Fly-back Converter for the Power Supply

Using the design procedure discussed in the previous section as a guide, the experimental converter was constructed using the following components: Transformer core: The core selected for the power Supply is UU 49/36/28 core. N87 MATERIAL AL = 3107nH, primary: 28T of 1 strands of 40/0.442 lit wire. Secondary: 48T of 2 strands, 37 of 1 strands, 3T of 1 strands, 3T of 1 strands, 2T of 1 strands, of 40/0.442lit wire, Lm: 2.45mH, Resonant

inductor: core: 58350-A2 winding: 42T of 3 strands of AWG 26 Lr: 127uH Clamp circuit: Cclamp: 16nF, and S2: APT4M120K MOSFET, S1: APT4M120K, UC1823AJ PWM Controller. Fig.13 shows the experimental waveforms of the gate-to-source voltages of main switch and auxiliary switch and the drain-to-source voltage of main switch. There is a time delay between the auxiliary switch turn-off and main switch turn-on to ensure main switch turn on at ZVS. Fig.14 gives the experimental waveforms of gate signals of main switch  $V_{gs}$  and auxiliary switch  $V_{ds}$  and transformer primary voltage  $V_{pri}$ . When main switch is turned on, the transformer primary side voltage is equal to  $V_{in}$ . If the main switch is turned off, the primary side voltage equals  $-nV_o = -326V$ . Fig.15 illustrates the measured results of gate signals  $V_{Smaings}$  and  $V_{Sauxgs}$  and clamped capacitor voltage  $V_{clamp}$ : When the auxiliary switch is turned on, the clamp capacitance is resonant with resonant inductance. Therefore the clamp voltage is resonant in this period. When the auxiliary switch is turned off, the clamp capacitor voltage is clamped to  $nV_o = 326$ .

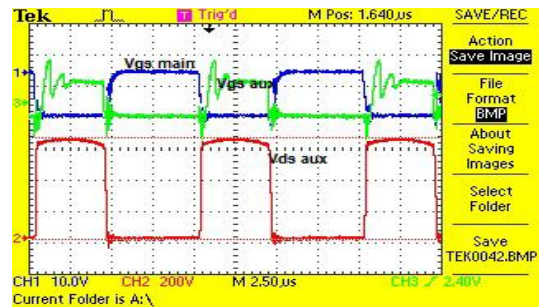


Fig. 13. Experimental waveforms of gate signals for main switch  $V_{gs}$ , and auxiliary  $V_{gs}$  and  $V_{ds}$ .

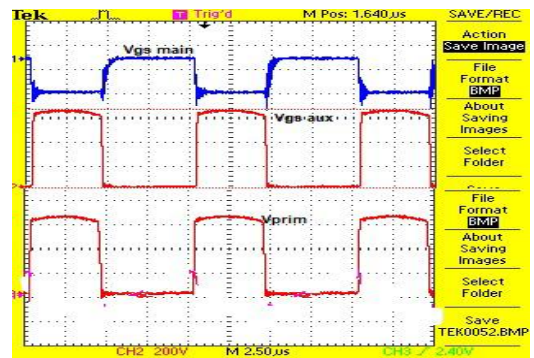


Fig. 14. Experimental waveforms of  $V_{gs}$  for main switch and auxiliary switch, and transformer primary voltage

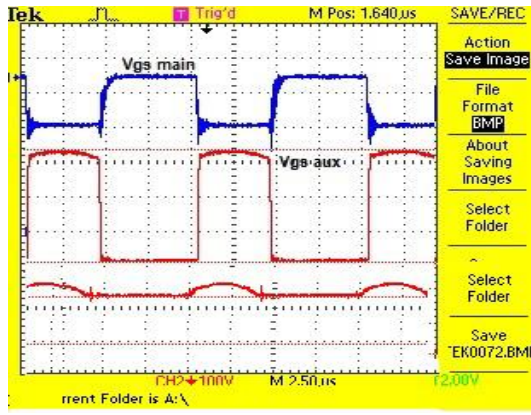


Fig. 15. Experimental waveforms of Vgs for main switch and auxiliary switch, and voltage across clamp capacitor

TABLE IV. ANALYSIS OF OUTPUT VOLTAGES OF POWER SUPPLY

Exper iment result from	O/P1	O/P2	O/P3	O/P4	O/P5	O/P6
output(V) required	9.6	403	303	15.5	15.5	15.5
Simulation	10.3	404	304	16.2	16.2	16.2
Hardware	9.6	403	303	15.5	15.5	15.5

## V. CONCLUSION

This paper gives a detailed circuit description, design and development, and experimental results of a soft-switched active clamp topology suitable for the power supply. The auxiliary clamp circuit is used to recycle the energy stored in the leakage inductance and suppress the voltage stress of main switch. The clamp circuit can also help the main switch to turn on at ZVS. Performance was experimentally verified for power supply. This result demonstrated that the active clamp variation of the traditional fly-back topology offers an attractive alternative to the more usual two-stage approach (boost cascaded by a buck) to off-line power conditioning for distributed power systems.

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