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Current Compensation using Modified Seven Level Multilevel Inverter and Fast Acting DC-Link Voltage Controller based DSTATCOM

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***Abstract*— The multilevel converter has drawn tremendous interest in the power industry. The general structure of the multilevel converter is to synthesize a sinusoidal voltage from several levels of voltages. Multilevel voltage source converters are emerging as a new breed of power converter options for high power applications. These converter topologies can generate high-quality voltage waveforms with power semiconductor switches operating at a frequency near the fundamental. Among the available multilevel converter topologies, the cascaded multilevel converter constitutes a promising alternative, providing a modular design that can be extended to allow a transformer less connection. A three-phase, seven level cascaded multilevel voltage source inverter with reduced number of switches based DSTATCOM for power line conditioning to improve power quality in the distribution network is used which will compensate the distorted line current harmonics and reactive power. The reference currents for generating switching signals of multilevel inverter are obtained using Instantaneous Real Power Theory. A new dc-link voltage controller is also used which will overcome the disadvantages of conventional Proportional Integral controllers.**

Keywords-DSTATCOM, Instantaneous real power theory, Proportional Integral controllers, Multilevel inverter, DC link capacitor.

I. INTRODUCTION

In recent years, many industrial applications have begun to require high power devices for their operations. As a result, the concept of multilevel converters was introduced as an alternative in high power and medium voltage situations. A multilevel converter is a power electronic system that synthesizes a desired output voltage from several levels of dc voltages as its inputs. Multilevel inverter output voltage produce a staircase output waveform which looks like a sinusoidal waveform. Multilevel converter technology started in the late 1960s with the introduction of the multilevel stepped waveform concept with a series-connected H-bridge, also known as cascaded H-Bridge (CHB) converter. This was followed by low-power development of a flying capacitor (FC) topology in the same year. Finally, in the late 1970s, the diode-clamped converter (DCC) was first introduced. The structure of separate dc sources is well suited for various renewable energy sources such as fuel cell , photovoltaic , biomass etc.[1]-[2].

Power quality problems have been experienced in distribution systems when connected to unbalanced and non linear loads [3]. Custom power devices like DSTATCOM can be connected in shunt to these systems for power factor correction, voltage regulation, current compensation, harmonic filtering etc. Multilevel inverters can be used with Flexible Alternating Current Transmission Systems (FACTS), custom power equipment and industrial drives.

Instantaneous real power theory [5]-[8] based multilevel inverter based DSTATCOM can be connected to the point of common coupling (PCC) through filter inductance to the distribution system [4]. The PI controller maintains the dc-bus voltage across the capacitor constant of the cascaded inverter. The instantaneous real-power compensator with PI-controller extracts reference value of current to be compensated.

A new multilevel inverter [9]-[10] which significantly reduces the number of dc voltage sources, switches and power diodes as the number of output voltage levels increases. To synthesize maximum levels at the output voltage, the proposed topology is optimized for various objectives, such as the minimization of the number of switches, gate driver circuits and capacitors, and blocking voltage on switches. The analytical analyses of the power losses of the proposed converter are also presented.

The capacitor across the multilevel inverter is designed, [11], which are used for the compensation of the reactive power. The design of the DC link capacitor is governed by the reduction in the DC bus voltage when loads are connected and increase in the DC bus voltage on removal of loads.

In this paper, a fast-acting dc-link voltage controller [12] based on the dc-link capacitor energy is proposed. The transient response of the conventional dc-link voltage controllers is slow, especially when the load changes rapidly. This disadvantage can be overcome using the new proposed dc-link voltage controller.

In this paper, a new DSTATCOM topology with reduced number of switches based multilevel inverter is proposed. The topology is designed for a seven level inverter which serves the purpose of the Voltage Source Inverter (VSI) in a DSTATCOM. The simulation studies are carried out using MATLAB/SIMULINK software, and results are presented in this paper.

II. DISTRIBUTION STATIC COMPENSATOR

The Distribution Static Compensator (DSTATCOM) is a shunt connected active filter which is connected at the Point of

Common Coupling (PCC) of the distribution system through a tie reactance. It mainly eliminates the power quality problems in currents. The main components of a DSTATCOM are three-phase inverter (MOSFET, Thyristor or IGBT) module, filter, dc capacitor and a control strategy. The basic electronic block is the voltage-sourced inverter that converts an input dc voltage into a three-phase output voltage at fundamental frequency. The DSTATCOM employs an inverter to convert the DC link voltage V_{dc} on the capacitor to a voltage source of adjustable magnitude and phase. The capacitor provides the dc link voltage which is charged with the power taken from the distribution network.

III. CASCADED MULTILEVEL INVERTER

A single phase, seven level configuration of the cascaded multilevel inverter is shown in Fig. 1. In a multilevel inverter, by increasing the number of output voltage levels the device voltage and the output harmonics can be reduced. Cascaded Multi-level inverter can avoid extra clamping diodes or voltage balancing capacitors which is present in diode clamped and flying capacitor multilevel inverters. The converter topology used here is based on the series connection of single phase inverters with separate DC sources.

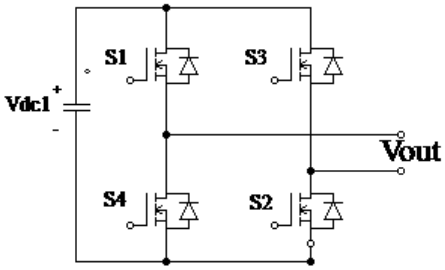


Fig. 1 A single H-bridge of cascaded multilevel inverter

IV. PROPOSED TOPOLOGY OF DSTATCOM

A closed loop, instantaneous real-power theory based cascaded multilevel inverter based DSTATCOM connected to a distribution system at the PCC through a filter inductance is shown in the Fig. 2. The main components of the system are-proposed multilevel inverter, RL-filters, a compensation controller (instantaneous real-power theory) and switching signal generator (proposed triangular-sampling current modulator). The three-phase supply source is connected to non-linear load and load currents contain fundamental and harmonic components. If the total reactive and harmonic power is provided by the active power filter, i_s (t) will be in phase with the utility voltage V_s(t) and it would be sinusoidal. At this time, the active filter provides the compensation current and it estimates the fundamental components and compensates the harmonic current and reactive power.

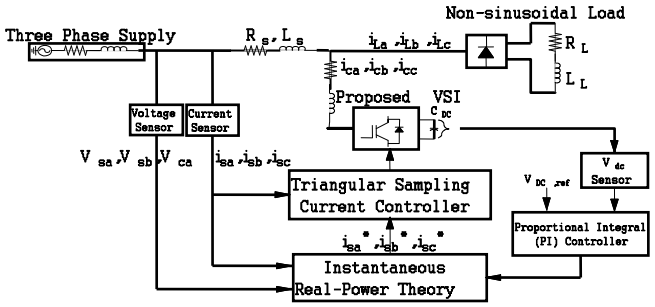


Fig. 2 Schematic Diagram of DSTATCOM

A. *Proposed Multilevel Inverter*

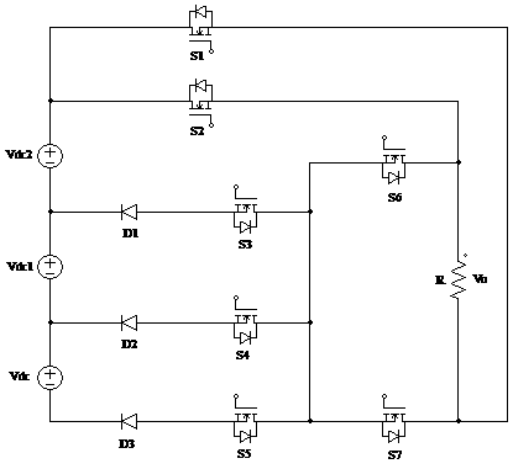


Fig. 3 Single Phase Circuit diagram of the Proposed Seven Level Multilevel Inverter

The proposed inverter [9]-[10] consists of seven switches and three separate DC sources with an R load as shown in Fig.3. The diodes are used for the protection of the switches. By switching the switches using firing pulses we can obtain the seven level output voltage. The inverter produces output voltage in seven levels: $+V_{dc}$, $+2V_{dc}$, $+3V_{dc}$, 0, $-V_{dc}$, $-2V_{dc}$ and $-3V_{dc}$. By turning on the switches according to the conditions in Table I, the various levels of output can be obtained. The Fig.4 shows the expected output waveform for the proposed inverter. When a switch S_2, S7 and S_3 are closed, the output voltage is $+V_{dc}$. When switches S_2, S7 and S_4 are closed, the output voltage is $+2V_{dc}$. When a switch S_2,S_7 and S_5 are closed, the output voltage is $+3V_{dc}$. Likewise, in order to obtain the negative amplitude of the output such as $–V_{dc}$, $-2V_{dc}$ and $-3V_{dc}$ switches S_1 and S_6 are switched by varying S_3,S_4 and S_5 alternatively. When no switch is operating output is 0. Therefore, to obtain the total ac voltage produced by the multilevel inverter, these seven distinct ac voltages are added together.

TABLE I.

TABLE II. SWITCHING CONDITIONS

Sl. No.	Conducting Switches	Amplitude of the Output Voltage
1	S_2,S_7,S_3	$+V_{dc}$
2	S_2,S_7,S_4	$+2V_{dc}$
3	S_2,S_7,S_5	$+3V_{dc}$
4	Nil	0
5	S_1,S_6,S_3	$-V_{dc}$
6	S_1,S_6,S_4	$-2V_{dc}$
7	S_1,S_6,S_5	$-3V_{dc}$

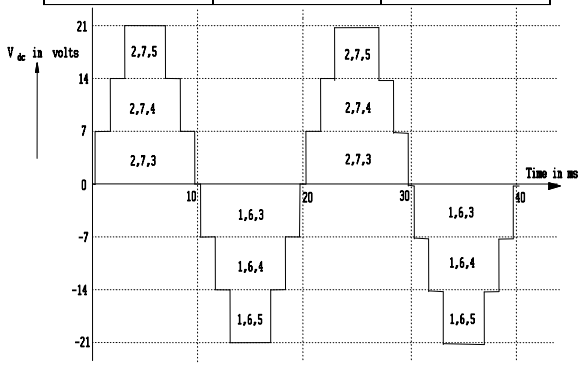
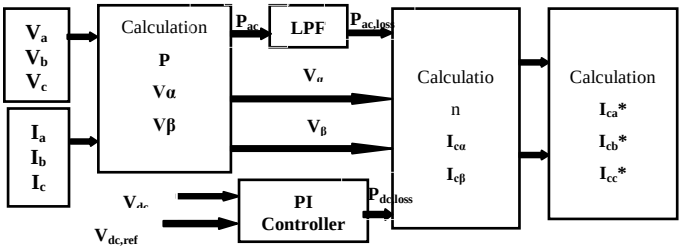


Fig. 4 Sample Output Waveform of the Proposed Multilevel Inverter

B. Reference Current Control Strategy

Fig. 5 Reference current generator using Instantaneous Real – Power Theory



Hirofumi Akagi [6] proposed a theory based on instantaneous values in three-phase power systems called as Instantaneous Power Theory or Active-Reactive (p-q) theory. It is valid for steady-state or transient conditions, as well as for generic voltage and current waveforms that allowing to control the active power filters in real-time. The active filter makes source current sinusoidal by supplying the oscillating portion of the instantaneous active current of the load.

The p-q theory[6]-[10] mainly consists of an algebraic transformation called Clarke's Transformation, by which three-phase voltages and currents in the *a-b-c* coordinates can be converted into voltages in α-β coordinates. The instantaneous space vectors voltage and current v_a, i_a are set on the a-axis, v_b , i_b are on the b axis, and v_c, i_c are on the c axis. The instantaneous source voltages v_{sa}, v_{sb}, v_{sc} are transformed into α, β coordinates voltage v_α, v_β by Clarke Transformation as follows:

$$\begin{pmatrix} v_\alpha \\ v_\beta \end{pmatrix} = \sqrt{\frac{2}{3}} \begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix} \begin{pmatrix} v_a \\ v_b \\ v_c \end{pmatrix} \quad (1)$$

$$\begin{pmatrix} i_\alpha \\ i_\beta \end{pmatrix} = \sqrt{\frac{2}{3}} \begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix} \begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} \quad (2)$$

The instantaneous real power (P_{ac}) defined in the α-β reference frame given by:

$$P_{ac} = v_\alpha i_\alpha + v_\beta i_\beta \quad (3)$$

For eliminating the higher order components this instantaneous real-power (P_{ac}) is passed to first order Butterworth design based 50 Hz low pass filter (LPF). It allows the fundamental component only. Ac components of the real-power losses are indicated using these LPF and it is denoted as $\overline{P_{ac}}$. The DC power loss is calculated by the comparing the dc-bus capacitor voltage of the proposed inverter with a reference voltage. The proportional and integral gains using PI Controller determines the dynamic response and settling time of the dc-bus capacitor voltage. The DC component power losses can be written as:

$$P_{DC(loss)} = \left[V_{dc,ref} - V_{dc} \right] \left[k_p + \frac{k_i}{s} \right] \quad (4)$$

The instantaneous real-power (P) is calculated from the AC component of the real-power loss $\overline{P_{ac}}$ and the DC power loss $P_{DC(Loss)}$. It can be defined as:

$$P = \overline{P_{ac}} + P_{DC(Loss)} \quad (5)$$

The instantaneous current on the αβ coordinates of $i_{c\alpha}$ and $i_{c\beta}$ are divided into two kinds of instantaneous current components; first one is real-power losses and second one is reactive power losses. But only the real-power losses can be calculated by this proposed controller. So the α,β coordinate currents $i_{c\alpha}$, $i_{c\beta}$ are calculated from the v_α, v_β voltages using only the instantaneous real power P and the reactive power q is assumed to be zero. This approach reduces the calculations and shows better performance than the conventional methods. The α,β coordinate currents can be calculated as shown below:

$$\begin{pmatrix} i_{c\alpha} \\ i_{c\beta} \end{pmatrix} = \frac{1}{v_\alpha{}^2 + v_\beta{}^2} \begin{pmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{pmatrix} \begin{pmatrix} P \\ 0 \end{pmatrix} \quad (6)$$

From this equation, the orthogonal coordinate's active-power current can be calculated. The α-axis instantaneous active current can be written as:

$$i_{c\alpha} = \frac{v_\alpha P}{v_\alpha{}^2 + v_\beta{}^2} \quad (7)$$

Similarly, the β-axis instantaneous active current can be written as:

$$i_{c\beta} = \frac{v_\beta P}{v_\alpha{}^2 + v_\beta{}^2} \quad (8)$$

Let the instantaneous powers P(t) in the α-axis and the β-axis represented as P_α and P_β respectively can be given by the definition of real-power as follows:

$$P(t) = v_{\alpha p}(t) i_{\alpha p}(t) + v_{\beta p}(t) i_{\beta p}(t) \quad (9)$$

From equation (9), substitute the orthogonal coordinates α-axis active current (7) and β- axis active current (8); we can calculate the real-power $P(t)$ as follows:

$$P(t) = v_\alpha(t)\left(\frac{v_\alpha P}{v_\alpha{}^2+v_\beta{}^2}\right) + v_\beta(t)\left(\frac{v_\beta P}{v_\alpha{}^2+v_\beta{}^2}\right) \quad (10)$$

The instantaneous real power P(t) generates the reference currents which is required to compensate the distorted line current harmonics and reactive power since it's AC and DC components are related to harmonic currents. The block diagram is as shown in Fig.5.

C. Triangular Sampling Current controller

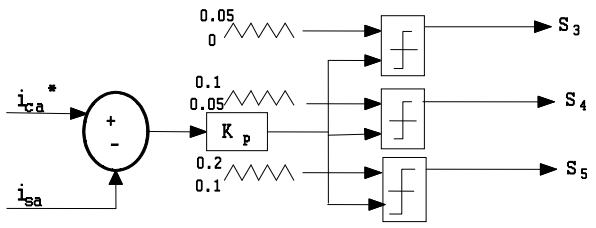


Fig. 6 Proposed triangular-sampling current controller

The triangular carrier current controller for active power filer applications generates gate control switching pulses for the switches S_3, S_4 and S_5 in the modified voltage source inverter. To determine the switching transitions by means the error current [desired reference current (i_a*) compared with the actual source current (i_a)] is multiplied with proportional gain (K_p). The output signal of the proportional gain is compared with triangular carrier signal. The triangular signals are of same frequency with different amplitude for multilevel inverter, because each phase in one converter does not overlap other phase shown in Fig.6. Each current controller directly generates the switching signal of the three A, B and C phases. The switching signals for S_1,S_6 and S_2,S_7 are generated using pulse generator.

V. DC LINK VOLTAGE CONTROLLERS

The dc link voltage will rise above its reference value when load is suddenly removed, but when the load is suddenly increased this dc link voltage is reduced below its reference value. As shown in Fig. 2, the source supplies an unbalanced nonlinear ac load directly and through the dc link of the APF it supplies a dc load. The dc bus voltage is significantly affected by the transients on load side and in order to control the dc link voltage, closed loop controllers are used. Proportional-integral-derivative (PID) controller provides a better solution to many control problems. The control signal used by PID controller to regulate the dc link voltage is as shown below:

$$U_c = K_p(V_{dcref} - V_{dc}) + K_i\int(V_{dcref} - V_{dc})dt + K_d\, d(V_{dcref} - V_{dc})/dt \quad (11)$$

Kp, K_i and K_d respectively are the proportional, integral, and derivative gains of the PID controller. When value of proportional controller gain is increased, the rise time and steady-state error reduces but it increases the overshoot and settling time. When integral gain is increased it reduces steady-state error but increases overshoot and settling time. Stability is improved by increasing the derivative gain. Practitioners have often found that the derivative term can behave against anticipatory action in case of transport delay, so it is switched off or even excluded. Therefore, PI controller based conventional and the proposed fast-acting dc-link voltage controller are given as follows:

A. Conventional DC-Link Voltage Controller

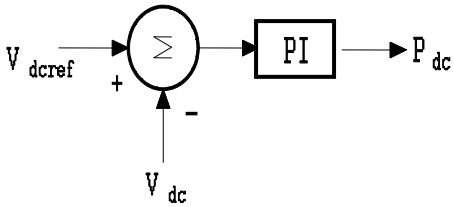


Fig. 7 Schematic Diagram of the Conventional Dc-Link Voltage Controller

The conventional PI controller used for maintaining the dc-link voltage is as shown in Fig.7. The real power required by the capacitor which is proportional to the difference between the actual and reference voltages to maintain the dc-link voltage at the reference value can be expressed as follows:

$$P_{dc} = K_p(V_{dcref} - V_{dc}) + K_i\int(V_{dcref} - V_{dc})dt \quad (12)$$

Since the capacitor voltage is sampled at every zero crossing of the phase supply voltage, the dc-link capacitor has slow dynamics compared to the compensator. For fast-changing loads, this conventional controller has slow transient response and dynamic response is dependent upon K_p and K_i values when P_{dc} is comparable to P_{lavg}. Also, the design parameters are quite difficult for a complex system and, hence, these parameters are chosen by trial and error method.

B. Fast-Acting DC Link Voltage Controller

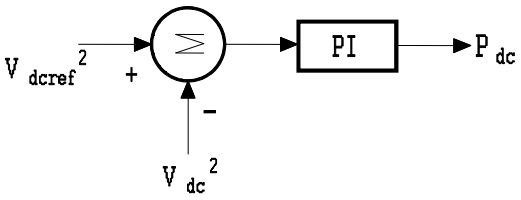


Fig. 8 Schematic Diagram of the New Fast-Acting Dc-Link Voltage Controller

To overcome the disadvantages of the conventional controller, an energy-based dc-link voltage controller is proposed. The energy which is required by the dc-link capacitor (W_{dc}) to charge from actual voltage (V_{dc}) to the reference value (V_{dcref}) can be obtained as follows:

$$W_{dc} = \frac{1}{2} C_{dc} (V_{dcref}^2 - V_{dc}^2) \quad (13)$$

The dc-link capacitor voltage has ripples with double frequency than that of the supply frequency. So the dc power ($P_{dc}^{'}$) required by the dc-link capacitor is given as:

$$P_{dc}^{'} = \frac{W_{dc}}{T_c} = \frac{1}{2T_c} C_{dc} (V_{dcref}^2 - V_{dc}^2) \quad (14)$$

where T_c is the ripple period of the dc-link capacitor voltage. This controller is as shown in Fig. 8 where the input to the controller is the error obtained between the squares of reference and the actual capacitor voltages and the total dc power required by the dc-link capacitor is computed as follows:

$$P_{dc} = K_{pe} (V_{dcref}^2 - V_{dc}^2) + K_{ie} \int (V_{dcref}^2 - V_{dc}^2) dt \quad (15)$$

where K_{pe} and K_{ie} are the proportional and integral gains of the energy-based dc-link voltage controller. This energy-based controller gives fast response compared to the conventional PI controller. So this can be called a fast-acting dc-link voltage controller. The proportional and integral gains can be calculated easily. The value of the proportional controller gain can be given as:

$$K_{pe} = \frac{C_{dc}}{2T_c} \quad (16)$$

The selection of K_{ie} depends upon the tradeoff between the transient response and overshoot in the compensated source current. It is found that if K_{ie} is greater than $K_{pe}/2$, the response becomes oscillatory and if K_{ie} is less than $K_{pe}/2$, then response becomes sluggish.

VI. Design of Conventional Controller Based on the Fast-Acting DC-Link Voltage Controller

The conventional dc-link voltage controller can be designed from the fast-acting dc-link voltage controller as:

$$P_{dc} = K_{pe} (V_{dcref} + V_{dc})(V_{dcref} - V_{dc}) + K_{ie} \int (V_{dcref} + V_{dc})(V_{dcref} - V_{dc}) dt \quad (17)$$

It can be also written as:

$$P_{dc} = K_p^{'} (V_{dcref} - V_{dc}) + K_e^{'} \int (V_{dcref} - V_{dc}) \quad (18)$$

where

$$K_p^{'} = K_{pe} (V_{dcref} + V_{dc}) \quad (19)$$

$$K_i^{'} = K_{ie} (V_{dcref} + V_{dc}) \quad (20)$$

From the above equations it can be observed that the gains of proportional and integral controllers vary with time. For very small ripples in the dc-link voltage, we can approximate the above gains to the following equations:

$$K_p^{'} \approx 2K_{pe} V_{dcref} \quad (21)$$

$$K_i^{'} \approx 2K_{ie} V_{dcref} \quad (22)$$

From these equations the approximate gains of conventional PI controller is obtained. Variation in V_{dc} is small during transient conditions. So $V_{dcref}+V_{dc}$ is not really equal to $2V_{dcref}$.

VII. Selection of DC Link Capacitor

The value of the dc-link capacitor is chosen such that it must have the ability to regulate the voltage under transient conditions. Let us assume that the compensator in Fig. 2 is connected to a system with a rating of X kilovolt amperes. The energy of the system is given by X×1000 J/s. A further assumption is made that the compensator deals with half (i.e. X/2) and twice (i.e.2X) capacity under the transient conditions for 'n' number of cycles with the system voltage for a period of Ts. Then, the change in energy that the capacitor has to deal is given by:

$$\Delta E = (2X - X/2) nT \quad (23)$$

Energy stored in the dc capacitor should support this change in energy. Let us allow the total dc-link voltage of the dc capacitor to change from 1.4Vm to 1.8Vm during the transient conditions where Vm is the peak value of phase voltage. So,

$$\frac{1}{2} C_{dc} [(1.8V_m)^2 - (1.4V_m)^2] = (2X - X/2) nT \quad (24)$$

which implies that

$$C_{dc} = \frac{3XnT}{(1.8V_m)^2 - (1.4V_m)^2} \quad (25)$$

VIII. Simulation Results

The load compensator with Proposed VSI topology as shown in Fig. 2 is realized using simulation done by using MATLAB. The system and compensator parameters are given in Table II. The load consists of a three-phase diode bridge rectifier feeding a highly inductive R-L load which is connected for the entire time period and an additional unbalanced load is also connected. The load and compensator are connected together at the point of common coupling (PCC). The source voltage and source currents are monitored and real power is computed. The matrix equations are solved to compute the reference compensator currents. The actual currents are then compared with the reference currents using triangular sampling current control. Based on the comparison, switching signals are generated. The source voltages and source currents are plotted without DSTATCOM in Fig. 10(a). The source current has total harmonic distortion of 26.29% as shown in Fig. 11(a). As seen from Fig. 10(b), the source current is balanced sinusoid when DSTATCOM is connected. The currents have a unity power factor relationship with the voltages in the respective phases. The THD in the source current is 4.65% as shown in Fig.11 (b).

TABLE II. Simulation Parameters

System Parameters	Values
Supply Voltage	415V(L-L), 50Hz
Non linear load	Three Phase Full wave rectifier

	feeding a R-L load of 30Ω-30mH
Unbalanced Non Linear load	Three Phase Full wave rectifier feeding loads such as: Z_a=1e5+0.314jΩ Z_b=50+ 318.3jΩ Z_c=1Ω
DC Capacitor	2020μF
Reference DC Link Voltage	650V
Gains of conventional dc link voltage controller	K_p=40 ,K_i=20
Gains of new fast acting dc link voltage controller	K_p=0.101 ,K_i=0.0505

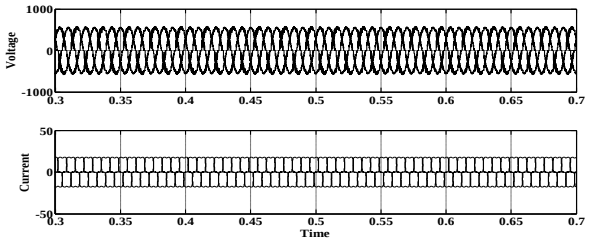


Fig. 10(a). Source Voltage and Current without DSTATCOM

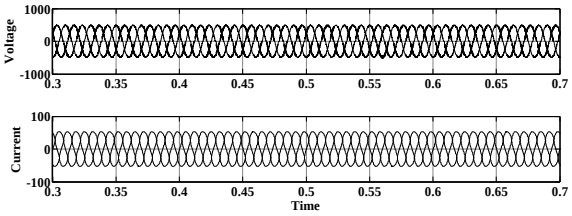


Fig. 10(b). Source Voltage and Current with DSTATCOM

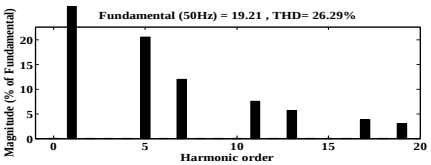


Fig 11(a). THD of source current without DSTATCOM

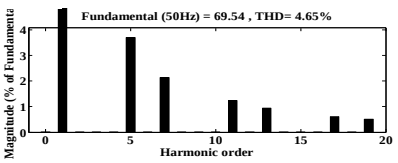


Fig 11(b). THD of source current with DSTATCOM

IX. CONCLUSION

A new cascaded converter with a minimum number of switches is proposed. This technology is suitable for high-voltage, high-power applications. A three-phase, seven-level modified converter is connected to an active filter for the compensation of source current when nonlinear loads are connected. For THD concerns, the proposed technique can be extended to have lower THD.

This paper has provided control theories for computing the reference currents and strategies for generating the switching signals for the operation of modified multilevel inverter based DSTATCOM. This project can be extended further by increasing the number of levels in new multilevel inverter by using lesser number of switches. Also the harmonic distortions can be reduced. Thus complexity in design can be minimized.

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