Bridgeless Dual Buck-Boost Converter Fed BLDC Motor Drive with Power Factor Correction

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Abstract – **BLDC motors are widely using in many of the industrial applications. Various converter topologies are used for feeding these BLDC motor drives.In this paper, a bridgeless configuration of buck boost converter is proposing. This converter offers good power quality at the AC mains with a filter performing the power factor correction. Speed control of the motor drive is performed by electronic commutation of the inverter switches. Simulation of this PFC bridgeless buck boost topology is done in MATLAB and the validity is proved.**

Keywords—Discontinous current conduction mode, Power factor correction,BLDC motor

I. INTRODUCTION

Brushless DC motors have got wide applications in the field of automobile vehicle technology, hard disc drives, compressors etc because of their high starting torque, reliable operation and good efficiency. Now a days various automobile applications are satisfied by these cost effective and reliable brushless technology operated motorsThese motors are actually permanent magnet AC motors resembling the torque-current characteristics of a DC motor. It is a modified form of Permanent Magnet Synchronous motor in which the back emf is trapezoidal which is sinusoidal in case of PMSM motors. Sensor and sensor less control are employed in BLDC motors, In sensor based control, the position of the rotor is identified by the Hall sensors which are provided at 120^0 apart. Since the technology is simple and highly reliable, BLDC motors are widely selecting in low power applications.

DC-DC converters are used for feeding these BLDC motor drives. Apart from the control of input voltage to the inverter driving motors, they are also performing the isolation between input and the load side. Various converter topologies are being used now a days depending on the requirements. Both bridge and bridgeless topologies are using, however the presence of diode bridge along with high value of DC link capacitor will lead to the reduction of power factor since the total harmonic distortion increases.Inverters are employed to supply power to the BLDC motor which is a three phase inverter. Voltage source inverters are most commonly using and the BLDC motor control through electronic commutation is made possible by controlling the gating sequence of inverter switches. Apart from these VSI, CSI and ZSI topologies are also employing.

Power quality issues are of great interest now adays. Most of the industrial applications are running with large power quality issues. Filters are usually provided along with these converters for the correction of power quality and thereby reducing the total harmonic distortion level.

The mode of operation of PFC converters are selected with great importance since it determines the cost and component ratings. Converters can be operated in both continuous conduction mode(CCM) and discontinuous conduction mode(DCM). DCM is mostly selecting in low power applications. This is because, for employing CCM it requires two sensors, one for sensing the inductor current and other for sensing the capacitor voltage. In DCM there requires only one sensor to detect the DC link voltage only. DC link voltage control cannot be selected in high power applications since it creates high stress on the switches

II. PROPOSED BRIDGELESS BUCK-BOOST CONVERTER FEEDING BLDC MOTOR DRIVE

The proposed system consisting of a bridgeless buck boost converter feeding a BLDC motor drive. The converter is operating in discontinuous inductor current mode for reducing the switching stress.An L filter is used at the input to improve the power quality. A dual buck boost converter is used in which one operating during positive half cycle and the other operating during the negative half cycle. In each of the half cycles, the DC link capacitor is continuously feeding the drive through three different modes. A voltage source inverter is used to provide alternating stator current to the motor drive. Electronic commutation is employed for controlling the switches of inverter so that the speed control of the BLDC drive can be made possible. Power factor correction is done by the voltage feedback control of the converter along with the filter operation. The switching stress will also be evaluated along with the other parameters so that the design of heat sinks can be done easily.

The circuit is operating in three modes in each of the half cycles.L_f and C_f are the filter inductance and capacitance at the input stage. S_{W1} and S_{w2} are the switches, L_1 and L_2 are the inductors, D_1 and D_2 are the diodes in the dual buck boost converter. The inverter switches are numbered through S_1 to S_6 and the BLDC motor drive employed with hall effect position (H_a-H_c) sensors are also shown in the circuit.

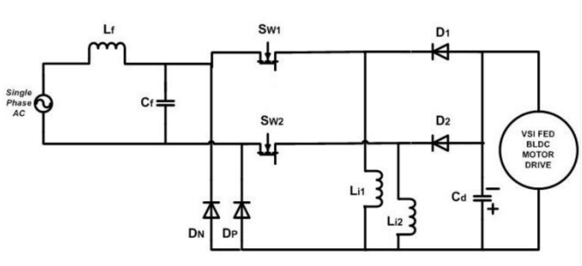

Fig 1 : Proposed Converter

III.OPERATION OF DUAL BUCK BOOST CONVERTER

The converter is a dual buck boost converter operating in both positive and negative half cycles of input supply voltage. It is performed in three different modes in each of the half cycles which is given below.

Operation during the positive half cycle

During this half cycle of operation the switch S_{w1} , inductor L_1 and the diodes $D_{p,}$ D_1 are operated to transfer energy from input to the load.

*Mode 1:*The switch S_{w1} is conducting and as result of this the inductor charges and the inductor current i_{L1} increases. The diode D_p completes the circuit. The previously stored charge in DC link capacitor will be transferred to the motor. It is shown in fig 1(a).

*Mode 2:*During this mode of operation, the switch S_{w1} turns off and the energy stored in inductor will be transferred to the DC link capacitor and the current i_{L1} will be decreased.. It is shown in fig 1(b).

*Mode 3:*In this mode none of the switch and the diode are conducting. The inductor enters into the discontinuous mode since the inductor current become zero. The energy stored in the DC link capacitor C_d will be transferred to the load. The Switch S_{w1} conducts again after the complete switching cycle.
Operation during the negative half cycle.. It is shown in fig 1(c).During this half cycle of operation the switch S_{w1} , inductor L_1 and the diodes $D_{p,}$ D_1 are operated to transfer energy from input to the load.

Operation during the positive half cycle

*Mode 1:*The switch S_{w2} is conducting and as result of this the inductor charges and the inductor current i_{L2} increases. The diode D_n completes the circuit. The previously stored charge in DC link capacitor will be transferred to the motor. . It is shown in fig 2(a).

*Mode 2:*During this mode of operation, the switch S_{w2} turns off and the energy stored in inductor will be transferred to the DC link capacitor and the current i_{L2} will be decreased.. It is shown in fig 2(b).

*Mode 3:*In this mode none of the switch and the diode areconducting. The inductor enters into the discontinuous mode since the inductor current become zero. The energy stored in the DC link capacitor C_d will be transferred to the load. The Switch S_{w2} conducts again after the complete switching cycle.. It is shown in fig 2(c).

During this half cycle of operation the switch S_{w2} , inductor L_2 and the diodes $D_{n,}$ D_2 are operated to transfer energy from input to the load.

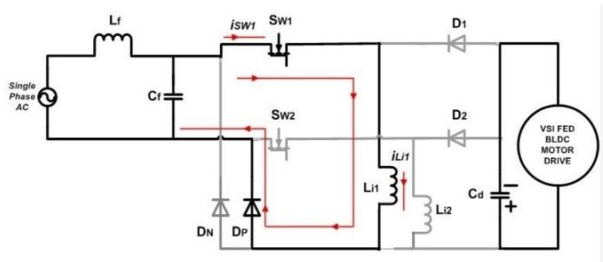

Fig 2 (a)

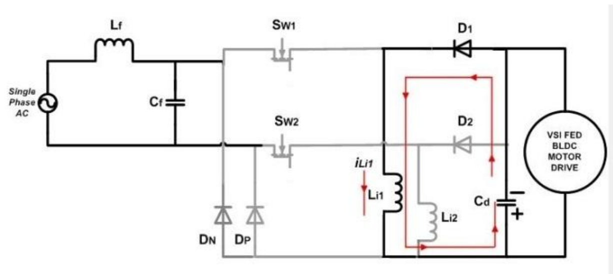

Fig 2(b)

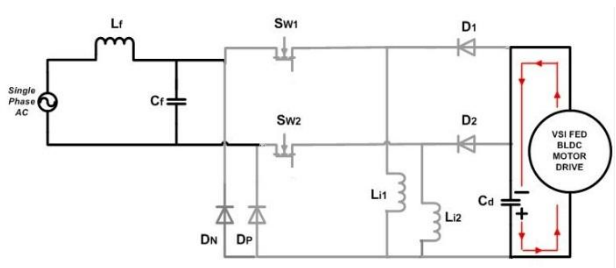

Fig 2(c)

Fig 2(a) : Mode 1 Fig2 (b): Mode 2 (c):Mode 3 operation of converter during positive half cycle

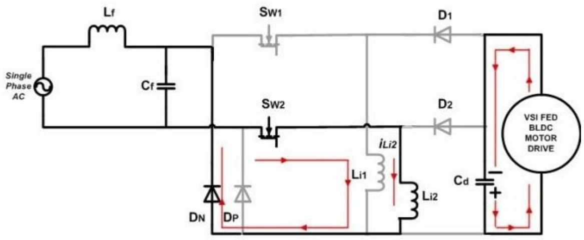

Fig 3(a)

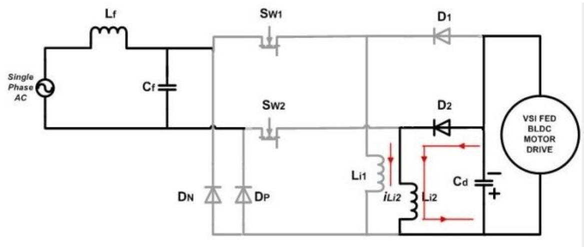

Fig 3(b)

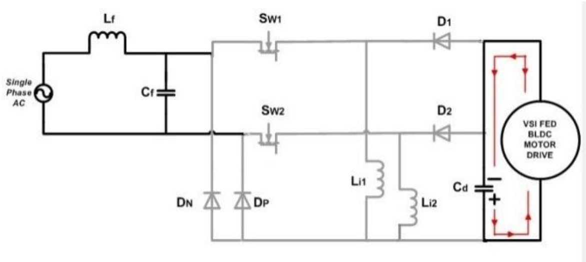

Fig 3(c)

Fig 3(a) : Mode 1 Fig 3(b):Mode 2 Fig 3(c):Mode 3 operation of converter during negative half cycle

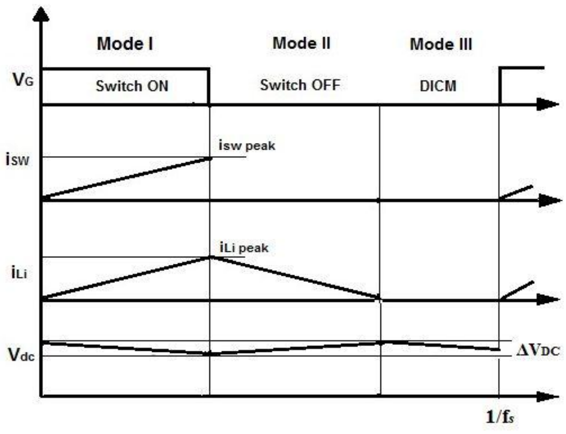

Fig 3.1 : Waveform representing mode operation in each half cycle

IV. DESIGN OF CONVERTER, FILTERPARAMETERS AND INVERTER SELECTION

The power factor corrected converter is operating in discontinuous inductor current mode such that the inductor currents L_{i1} and L_{i2} become discontinuous in a switching period. The BLDC motor used is of power 250W and the converter is designed for a rating of output power 350W. The RMS value of input voltage is 220V.

$$V_{in} = \frac{2\sqrt{2}Vs}{\pi} = \frac{2\sqrt{2}*220}{\pi} = 198V$$

The converter is designed from 50V to 200V with a nominal voltage of 100V. So the duty cycle might varies from .2016 to .5026

A) Design of input inductors L_{i1} and L_{i2}

For a converter operating in crictical conduction mode the value of Inductance is given by

$$L_{i1,2} = \frac{R\ (1-d*d)}{2fs}$$

The converter operates in very low value od duty ratio. At minimum duty ratio the converter is operating at 50V and 90W power.

$$L_{i1,2} = \frac{Vdcmin\ *Vdcmin\ \ (1-d*d)}{Pmin\ *2fs} = \frac{50*50\ (1-.2016*.2016)}{90*2*20000}$$

= 442.67µH

This can approximately be selected as 300µH. For the reliable operation in DICM mode 1/10 of this value is taken. So its value become 30µH.

B) Design of DC link capacitor C_d

For designing, the amount of second order harmonic current flowing through the capacitor should be taken into consideration.For a nominal value of 100V, thepermitted ripple in the DC link voltage can be taken of the order of 3%

$$C_d = \frac{Id}{2w\Delta Vdc} = \frac{Po/Vdc}{2w\Delta Vdc} = \frac{350/10}{2*314*.03*100} = 1857.7\ \mu F$$

Therefore the nearest possible value for the DC link capacitor can be selected as 2200 µF.

C) Design of input filter

A second order low pass LC filter is used to absorb the higher order harmonics in order to avoid it from the supply current. The value of capacitor is designed such that

$$C_{max} = \frac{Ipeak\ \tan(\alpha)}{\omega L*Vpeak} = \frac{350*1*\tan\ 1}{220*220*1.732*314} = 401.980\ nF$$

So the value of capacitor selected is 330nF.The required value of inductance is given by

$$L_{req} = L_f - L_s$$

Where L_f is the inductance of the filter and L_s is 4-5% of the base impedance.

$$L_{req} = \frac{1}{4\pi\pi*fc*fc*Cf} - 0.04*\frac{1*220*220}{314*350} = 1.57mH$$

So a low pass filter with capacitance 330nF and inductance 1.6mH is to be selected.

D) Selection of Inverter for feeding BLDC drive

A voltage source inverter is selected to feed the BLDC motor drive. It is a 6 switch inverter in which three legs are used to align them as upper and lower leg switches. One switch from upper and one from lower are active at a particular instant of time. The inverter switches are gated such that the stator voltages should be within the rating of motor selected.

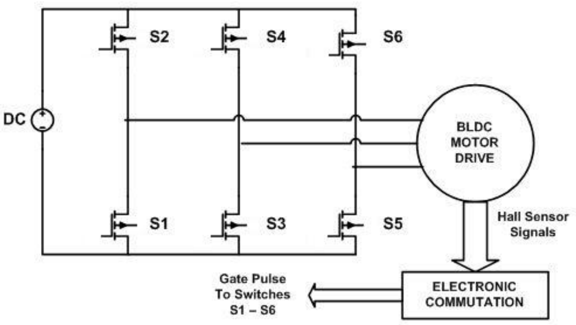

Fig 4 : Voltage Source Inverter feeding BLDC Motor

V. CONTROL OF POWER FACTOR CORRECTED BRIDGELESS BUCK BOOST CONVERTER

A) Control of PFC Converter

The converter is operating in DICM mode and it is being controlled by voltage follower approach. The PWM signals to the switches S_{w1} and S_{w2} are generated by comparing the DC link voltage with a referenca signal.The reference signal is generated such that

$V_{dc}^{*} = k_v w^{*}$

wherek_v is the motors voltage constant and w^* is the reference speed. The error signal is generated by comparing this DC link voltage level with the reference DC link voltage.

$V_e = V_{dc}^{*} - V_{dc}$

This error signal is given to the PI controller to produce the control output voltage.This output control voltage is compared with a sawtooth wave of high frequency (m_d) to generate the PWM pulses.

If $V_s > 0$,

If $m_d < V_{cc}$, then S_{w1} ON
If $m_d \geq V_{cc}$, then S_{w1} OFF

If $V_s < 0$,

If $m_d < V_{cc}$, then S_{w2} ON
If $m_d \geq V_{cc}$, then S_{w2} OFF

S_{w1} and S_{w2} are the switching signals.

B) Electronic Commutation

Electronic commutation is performed with proper switching of the VSI switches such that symmetrical current is taken from the DC link capacitor for 120^0 and placed symmetrically at each phase. Hall effect position sensor is required to determine the rotor position. Depending upon this, the gating signals to the inverter switches are produced by means of a decoder and corresponding switches from the upper and lower leg are activated to complete the current flow and thereby actuating the stator windings.

Fig. shows the case of line current i_{ab} drawn from the DC link capacitor whose values depending on the V_{DC} voltage along with the emfse$_{an}$,e$_{bn}$, resistance R_a,R_b and the inductances L_a,L_b and M. Table shows the switching sequence of VSI along with the status of hall effect position sensors.

The frequency of the hall sensors are not same. Their variation in active states are decoded for making the following switching sequence. The upper leg switches should provided with a bootstrap oriented gate control since the switch is connected in the higher voltage side.

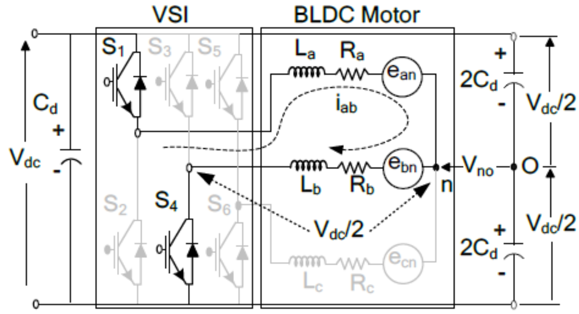

Fig 5 : Operation of BLDC motor when switch S1 and S4 are conducting

TABLE 1: Switching states foe achieving electronic commutation based on hall sensor output signal levels

Hall Signals			Switching Sequence					
H_a	H_b	H_c	S_1	S_2	S_3	S_4	S_5	S_6
0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	1
0	1	0	0	1	1	0	0	0
0	1	1	0	0	1	0	0	1
1	0	0	0	0	0	1	1	0
1	0	1	1	0	0	1	0	0
1	1	0	0	1	0	0	1	0
1	1	1	0	0	0	0	0	0

VI.SIMULATION RESULTS

The performance of proposed BLDC motor drive is simulated in MATLAB/Simulink environment using the Sim-Power-System toolbox. The performance evaluation of theproposed drive is categorized in terms of performance of BLDC motor, BL buck boost converter and the achievedpower quality indices obtained at AC mains. The parametersassociated with BLDC motor such as speed,electromagnetic torque and the stator current areanalysed for proper functioning of BLDC motor. Parameterssuch as supply voltage, supply current, DC linkvoltage, inductor currents, switch voltages and switches currents of PFC BL buck boost converter are evaluated to demonstrate its proper functioning. Moreover, power quality indices such as PF (Power Factor), DPF (Displacement Power Factor), CF (Crest Factor) and THD (Total Harmonics Distortion) of supply current are analysed for determining power quality at AC mains.

The simulation results are shown below. The performance of the motor under two different speeds are analysed. Satisfactory performances are obtained from the motor performance analysis. Power quality is maintained and various simulation results are shown below.Fig. 6(a) and 6(b) shows simulation result of the speed and DC link voltage level corresponding to a reference speed of 1000 rpm.

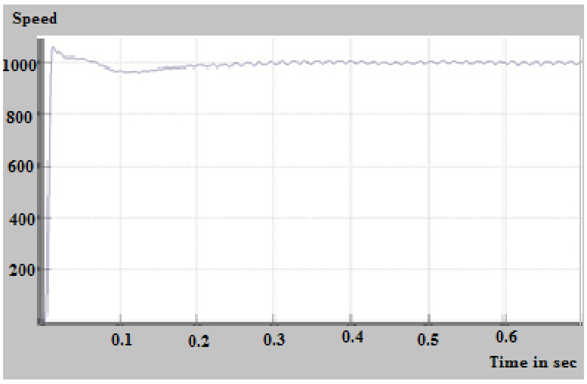

Fig 6(a): Speed control for a reference speed of 1000 rpm

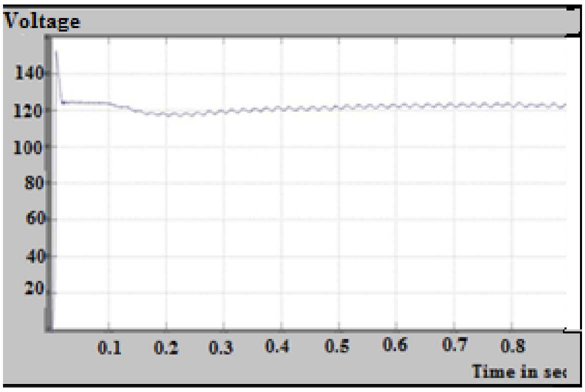

Fig 6(b) : DC link voltage level at 1000rpm

Fig. 7(a) and 7(b) shows simulation result of the speed and DC link voltage level corresponding to a reference speed of 1400 rpm.Fig 8 gives the rotor positions at different instants which show that the motor is running continuously. Fig 9gives the variation of torque at different angular positions of the rotor. Fig 10 shows the inverter phase voltage which is required for running the motor.

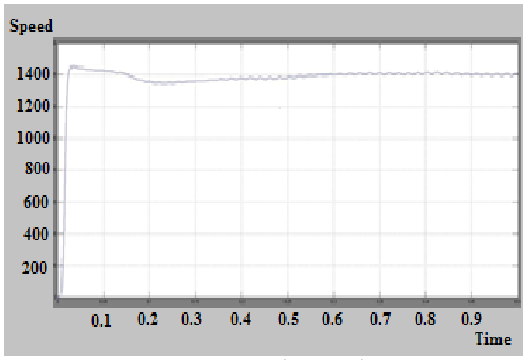

Fig 7(a): Speed control for a reference speed of1400 rpm

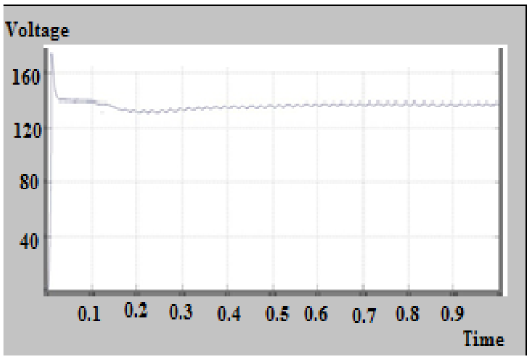

Fig 7(b) : DC link voltage level at 1400 rpm

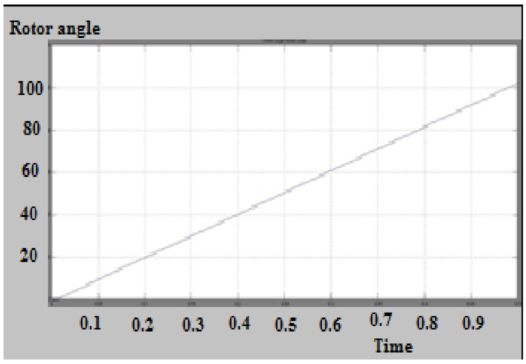

Fig 8: Rotor angle positions at a reference speedof 1400 rpm

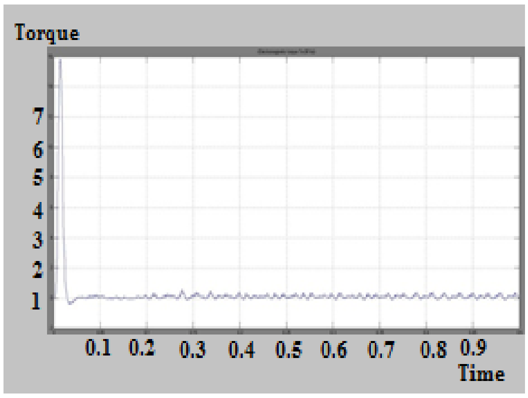

Fig 9: Torque of motor at a reference speed 1400 rpm

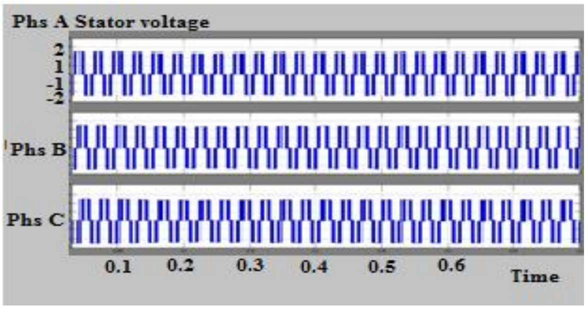

Fig 10: Three phase inverter output voltages fed to stator windings

The power quality at the AC mains can be checked by analysing the input voltages and currents. Fig 11 shows the input voltage and current waveforms.The improvement in the power factor can be detected from Fig 12, in which it reaches near to unity from a lower level of 0.66, shows the correction in power factor.

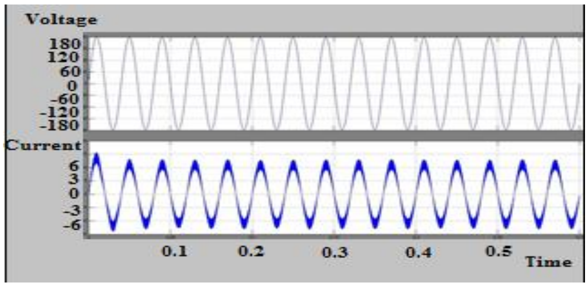

Fig 11:Input voltage and current waveform

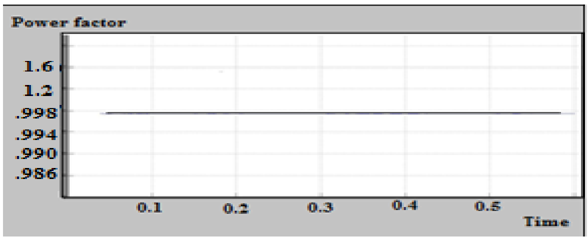

Fig 9 : Power factor after power quality control

VII. CONCLUSION

This paper presents the simulation of bridgeless dual buck boost converter operating in DICM, feeding a BLDC motor drive in low power applications. With this proposed converter the power quality can be improved at the AC mains. The total harmonic distortion can be reduced by using a low pass filter at the input.The power factor can be improved upto 0.98 with this arrangement. The speed control of the BLDC motor can be carried out by varying the DC bus voltage level. Electronic commutation will leads to the reduction of switching stress in the inverter. Speed can be controlled by the variation in DC link voltage. Since converter operating in DICM mode, no need to adopt current control mode which require more number of sensors and also an inner current loop.

Future scope includes the introduction of any isolation network to control the undesired flow of electric current and a dynamic load change analyser can be used for detecting rapid load changes..

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