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A New ZVS Full Bridge DC-DC Converter

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***Abstract*—Soft-switching techniques are used for efficiency improvement by reducing voltage stress across switch.The switches get turn on and turn off at zero voltage.Thus, the switching power losses are eliminated.It is obtained by adding resonant components including inductors and capacitors.The Zero voltage switching range can be increased by adding inductance in series with the transformer.It is seen that ZVS range is gained for no load to full load conditions.**

Keywords—zero voltage switching,full bridge converter,phase shift

I. INTRODUCTION

Full-bridge converters are commonly used in medium to high power dc-dc power conversion.High power density, high efficiency and high reliability are the most desirable features of this topology. For power levels up to 3 kW, MOSFET's are used to implement full bridge converters.

Soft-switching techniques are used for efficiency improvement by reducing voltage stress across switch.The switches get turn on and turn off at zero voltage and current.Thus, the switching power losses are eliminated.It is obtained by adding resonant components including inductors and capacitors.Soft-switching can be provided using either ZCS or ZVS technique. In most of these converters zero voltage switching (ZVS) is achieved by placing a snubber capacitor across each of the switches and either inserting a series inductor or parallel inductor with the transformer [1]-[3].In DC-DC full bridge converter,the snubber capacitor may be the internal capacitor of the MOSFET.In order to get zero current operation, a resonant inductor (Lr) is added in series with the switch.

The right and left legs of the bridge are operated with a phase shift.Phase-shifted topology provides ZVS turn on.Thus switching losses can be eliminated. In the full bridge topology,the opposite switches makes a freewheeling stage by means of phase shift.The absence of dead time between the turn-OFF and the turn-ON of the MOSFET switch in the same leg would lead to shoot through with switching losses.

A major demerit of this approach is the dependency of the ZVS characteristic on load.The full bridge dc-dc converter's ZVS capability will loose in the light load.Hence auxiliary connected inductors are provided to enable the ZVS condition which is independent to the load [4-6].

II. DESCRIPTION OF THE CIRCUIT

Fig.1 shows the DC-DC full-bridge converter.It consists of power circuit and auxiliary circuit.

The power circuit consists of:

i. S1,S2,S3,S4 MOSFET switches.
ii. Isolation Transformer.
iii. Diode bridge rectifier.
iv. Lf,output filter.
v. R0,Load

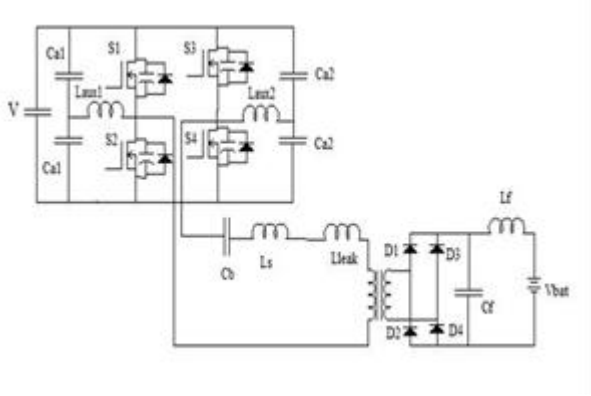

Fig.1.Phase shifted DC-DC Full-bridge converter

The auxiliary circuit consists of:

i. Ca1 and Ca2,capacitive voltage divider.
ii. Laux1 and Laux2,auxiliary inductors.
iii. Cso, drain-source snubber capacitors across switches.

A. Steady state Analysis

The assumptions to simplify the analysis of the steady state are given below

(i) Constant dc input voltage VBUS, and output

dc voltage Vo.

(ii) Output power,Po is constant.

iii)The Delay time between the two switches of the same leg of the bridge.

(iv) The Phase shift between the diagonal switches of the bridge.

(v) Ca1 and Ca2 have equal capacitance.

The proposed converter has seven modes of operation.

B. Circuit Analysis

Circuit analysis of ZVZCS full-bridge dc-dc converter is done.There are seven modes of operation.Here mathematical modeling is carried out. A model may help to study the effects of different components and to make predictions about their behaviour.

Mode 1:($t_0 \le t \le t_1$): At t_0 , S2 is turned OFF. The output capacitor of S1 is discharging and that of S2 is charging up with the reactive current provided by the auxiliary circuit. During this interval, the secondary-side diodes are reversed biased and are OFF. Therefore, the rising voltage Vab conducts a very small current through the DC blocking capacitor Cb, series inductance Ls , leakage inductance Lleak , and magnetizing inductance LM . The current through the series inductance.

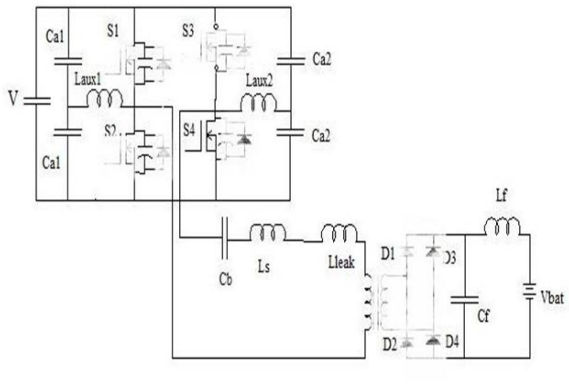

Fig.2. Mode 1 operation of full bridge converter

The current through Ls ,

$$i_s(t) = \frac{1}{L_S + L_{leak} + L_m}\int_0^t V_{AB} \qquad (1)$$

$$V_{AB}(t) = V_{dc} - V_{cs0}(t) \qquad (2)$$

$$V_{AB} = \frac{Q}{C} = \frac{I \times t}{C} = \frac{I_{PA}}{C_{S0}}(t - t0) \qquad (3)$$

$$i_s(t) = \frac{I_{PA}}{4(L_S + L_{leak} + L_m)C_{S0}}(t - t_0)^2 \qquad (4)$$

Current through auxiliary inductor is given by,

$$i_{aux}(t) = \frac{-V_{dc}}{4L_{aux}}(t_1 - t_0) + I_{aux} \qquad (5)$$

Since S2 turned off $I_{aux\,1}$ reaches maximum value. Then gradually inceases.

Mode 2 ($t_1 \le t \le t_2$): The output capacitor of the MOSFET, S1 is still discharging to finally reach zero and that of S2 is charging up to Vdc . Thismode ends once the voltage across this capacitor becomes zero. This interval ends once the output capacitor of the MOSFET S1 , has discharged completely.

Current flow through series inductor , is calculated as

$$i_s(t) = \frac{1}{L_S + L_{leak}}\int_{t0}^{t} V_{AB} - K(V_0 + 2V_d)dt \quad (6)$$

$$= \frac{1}{L_s + L_{leak}}\int_{t0}^{t} \frac{I_{PA}}{2C_{s0}}(t - t_1) - K(V_0 + 2V_d)dt \qquad (7)$$

$$= \frac{I_{PA}}{4(L_S + L_{leak})C_{s0}}(t - t_1)^2 - \frac{K(V_0 + 2V_d)}{L_s + L_{leak}}(t - t_1) \qquad (8)$$

Current through auxiliary inductor is given by,

$$i_{aux}(t) = \frac{-V_{dc}}{4L_{aux}}(t_2 - t_0)(9)$$

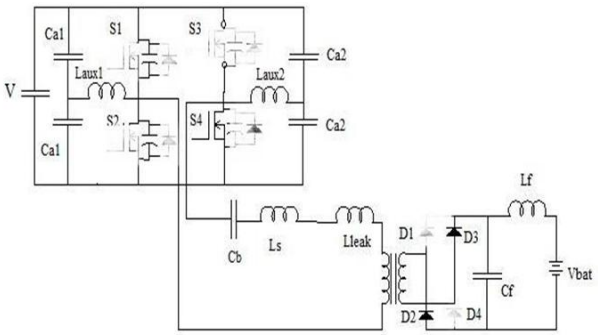

Fig.3. Mode 2 operation of full bridge converter

MODE 3($t_2 \le t \le t_3$): This mode starts once the MOSFET output capacitors have been charged and discharged completely.During this mode, the output diodes clamp the secondary voltage to the output voltage. Thus, there is a constant voltage across the combination of the series inductance and the leakage inductance.Therefore, the series current ramps up to its peak value.This mode ends once the MOSFET S4 , gate voltage becomes zero.
Current through series inductor is given by,

$$i_s(t) = \frac{1}{L_s + L_{leak}}\int_{t0}^{t} V_{dc} - K(V_0 + 2V_d)dt \qquad (10)$$

$$i_s(t) = \frac{V_{dc} - K(V_0 + 2V_d)}{L_s + L_{leak}}(t - t_2) \qquad (11)$$

$$= \frac{I_{PA}}{4(L_S + L_{leak} + L_m)C_{s0}})(t - t_1)^2 - \frac{K(V_0+2V_d)}{L_s + L_{leak}}(t - t_1) \quad (12)$$

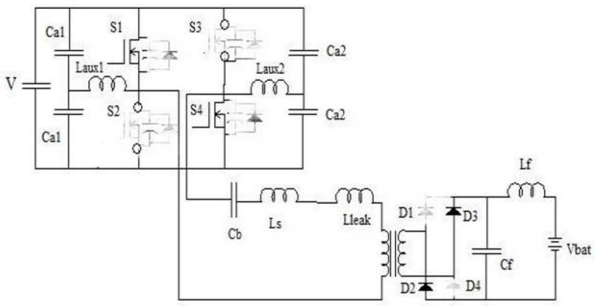

Fig.4. Mode 3 operation of full bridge converter

Mode 4 ($t_3 \leq t \leq t_4$): During this interval the output capacitor of S3 is discharging from and that of S4 is charging up to Vdc.This mode ends once the S3 output capacitor got completely discharged and S4 output capacitor got charged to Vdc .

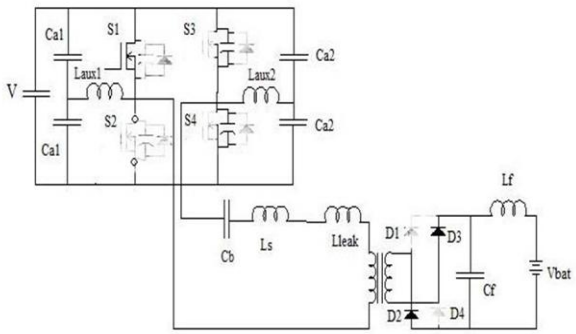

Fig.5. Mode 4 operation of full bridge converter

Mode 5 ($t_4 \leq t \leq t_5$): During this mode, the output voltage of the inverter is zero and the output diodes clamp the secondary voltage to the output voltage. Thus, a net negative voltage is incident across the series inductor, which is the reflected output voltage at the transformer primary side.This interval is part of the dead time between the gating pulses of S3 and S4.

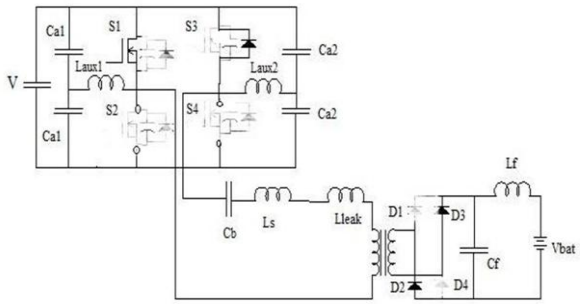

Fig.6. Mode 5 operation of full bridge converter

Therefore, in this mode the body diode of S3 is conducting. Once the gate pulse of S3 is applied this mode finishes and the current flows through the MOSFET channel.

Series current is given by,

$$i_s(t) = i_s(t4) - \frac{K(V_0+2V_d)}{L_s+L_{leak}}(t - t4) \quad (13)$$

Mode 6 ($t_5 \leq t \leq t_6$): This mode starts when the gate pulse is applied to S3.The equivalent circuit is the same as the previous mode except S3 channel is conducting in this mode rather than the body diode of S3. Therefore, the series inductor current is still ramping down to reach zero at the end of this mode. It should be noted that S1 turns off under near zero current switching at the end of this mode. At the end of this mode, the current through the series inductor reaches zero, so that the output diodes D2 and D3 naturally turn off with zero current.

$$i_{aux}(t) = \frac{V_{dc}}{2L_{aux}}(t6 - t5) \quad (14)$$

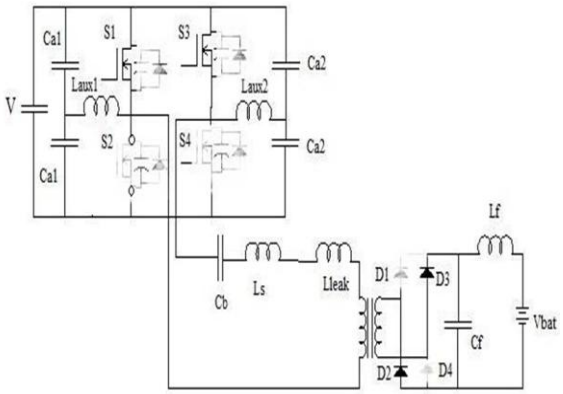

Fig.7. Mode 6 operation of full bridge converter

Mode 7 ($t_6 \leq t \leq t_7$):This interval starts once the current through output diodes reaches zero and the diodes naturally turn offwith zero current.During thismode, the output capacitor Cf feeds the output load with its stored energy while on the transformer primary side there is no current.

$$i_{aux}(t) = \frac{V_{dc}}{2L_{aux}}(t7 - t6) \quad (15)$$

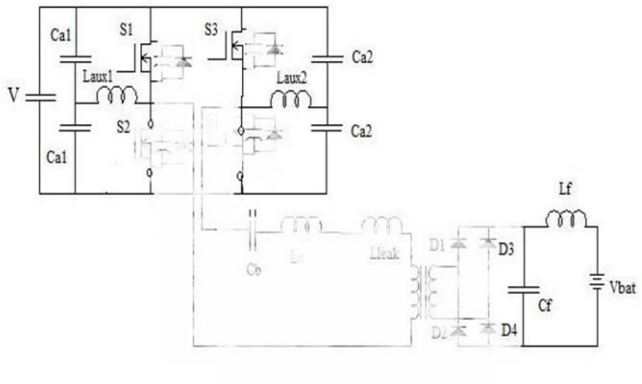

Fig.8. Mode 7 operation of full bridge converter

CONCEPT OF ZERO VOLTAGE SWITCHING

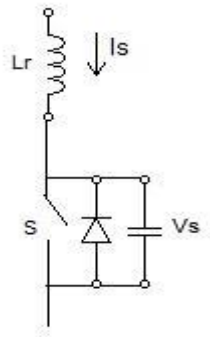

Fig.9. Resonant switch

Figure shows the resonant switch functions in ZVS condition.A resonant capacitor is connected across the switch otherwise known as parasitic capacitance.I nitial stage the switch is in off condition.This time the voltage across the switch is zero.When we switch on in zero voltage condition current flows in reverse direction through the channel of MOSFET.Now we want to switch off.When current flows through the MOSFET,voltage across the switch is zero.

When we switch off,the voltage across the capacitor diminish slowly but current become zero and the switch gets off.The voltage across the switch as well as capacitor become zero.The voltage across the switches S1 and S4 shows in waveform.The capacitor across S2 will be charged to (Vdc/2) and the capacitor across S1 discharged to zero.During the delay time,the capacitor across S1 discharged completely.Then polarity across capacitor of S1 changed.Now the body diode across S1 will conduct and switch S1 gets on at zero voltage.

DESIGN PROCEDURE

A. Design of Auxiliary inductor

Auxiliary inductor works as a constant current source.Further it discharge the capacitor across switch 2.

Maximum current through the inductor is,

$$I_{AUX} = \frac{V_{dc}}{8f_s L_{AUX}} \quad (16)$$

The inductor value is,

$$L_{AUX\,1} = \frac{V_{DC}\,T_D}{16F_S C_{S1}(V_{DC}+V_Z)} \quad (17)$$

To design the auxiliary inductor,the energy is calculated charge and discharge the snubber capacitor [5].This value is,

$$W_{Cs} = C_{s2}{V_{dc}}^2 \quad (18)$$

The stored energy in auxiliary and the leakage inductor are,

$$W_L = \frac{1}{2}L_{leak}{I_p}^2 + \frac{1}{2}L_{AUX\,2}{I_{AUX\,2}}^2 \quad (19)$$

The peak current value of the auxiliary inductor is,

$$I_{AUX} = \frac{V_{dc}}{8f_s L_{AUX}} \quad (20)$$

The value of auxiliary inductor is,

$$L_{AUX2} = \frac{1}{128{f_s}^2 C_{s2}} \quad (21)$$

B.Design of Series Inductor

In critical conduction mode,average current through inductor is half of the peak value of current flowing through the inductor [5],[7].

The value of the series inductor is,

$$L_{seq} = (1 + K\frac{V_0}{V_{dc}})\frac{{V_0}^2}{P_{0max}}\frac{T_s}{64} \quad (22)$$

C.Design of output capacitor

Capacitor is designed such a way that it can work in the maximum load of the converter.Minimum value of the capacitor is designed in a peculiar way that in peak load also the capacitor functions.

Capacitor designed as,

$$C_f = \frac{I_0}{f_s \Delta V_{cf}} \quad (23)$$

EXPERIMENTAL RESULT

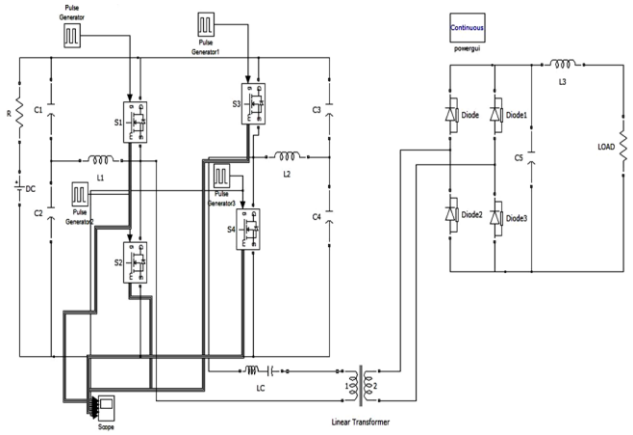

Fig.11. Open loop simulation circuit of full bridge dc-dc converter

Figure11 shows the open loop simulation circuit of full bridge dc-dc converter.There are four switches provided.To trigger these switches,pulse generators are provided.The phase shift of the diagonal switches and the legs of the same switches are having delay time.Gate signal is provided according to the delay to avoid short circuit.G1 is the gate signal through switch S1.G2 signal is the half time period of G1 added with a delay time.G3 is one-third time period of G1.Half plus one-third time period of gate signal 1 is given as fourth pulse. Before applying gate pulse,voltage across the switch S4 is made zero.Thus zero voltage switching turn on is possible.

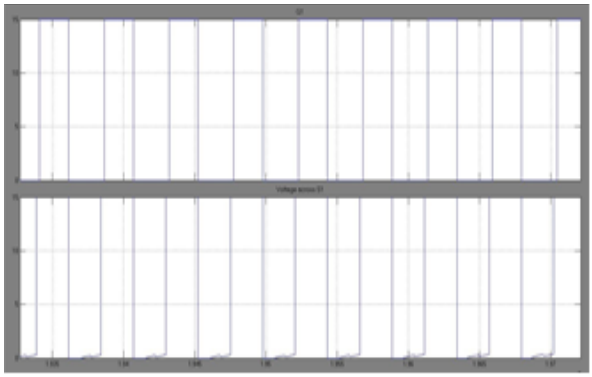

Fig.12. Zero voltage switching across switch S1

Figure 12 shows zero voltage switching achieves in open loop. Figure 13 shows ZVS in mode 6

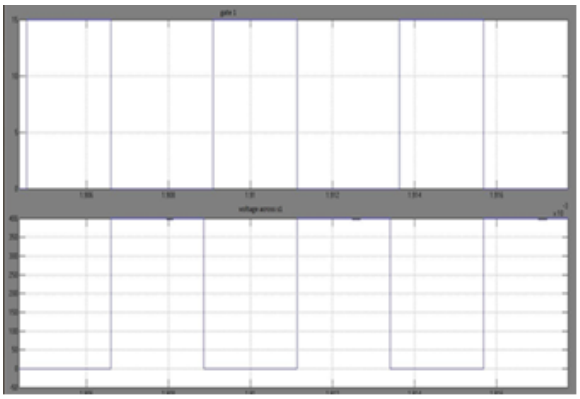

Fig.13. Zero voltage switching across switch S4

Before applying gate pulse,voltage across the switch S1 is made zero.Thus zero voltage switching turn on is possible.

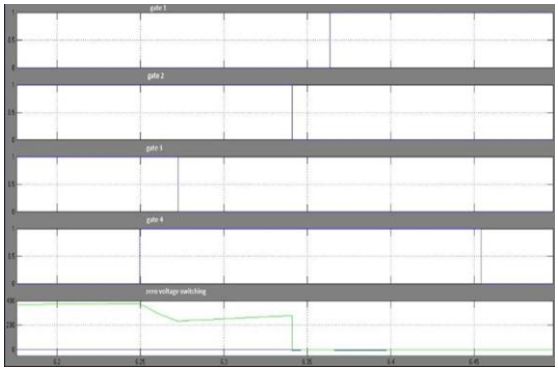

Fig.14. Zero voltage switching in mode 6.

To convert open loop to close loop,compare the DC voltage with constant output voltage,Which is given as inputto PI controller and it's output is given to PWM DC to DC generator.The output of the PWM generator is given to four MOSFET switch as gate signal. As the diagonal switches S1 and S4 on,we get positive output voltage +VABand regarding diagonal switches S2 and S3 on,we get -VAB.When both upper switches or lower switches on.we get zero voltage. Before applying gate pulse,voltage across the switch S1 is made zero.Thus zero voltage switching turn on is possible. Before applying gate pulse,voltage across the switch S4 is made zero.Thus zero voltage switching turn on is possible.

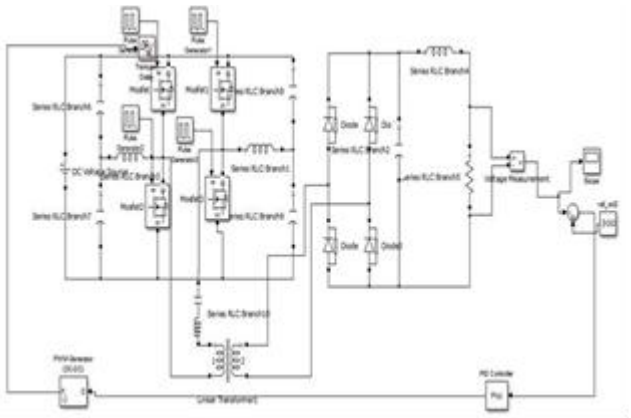

Fig.15.Closed loop circuit of the DC-DC full bridge converter

Figure14 shows the closed loop simulation circuit of full bridge dc-dc converter.The phase shift of the diagonal switches and the legs of the same switches are having delay time.Gate signal is provided according to the delay to avoid short circuit.G1 is the gate signal through switch S1.G2 signal is the half time period of G1 added with a delay time.G3 is one-third time period of G1.Half plus one-third time period of gate signal 1 is given as fourth pulse. Before applying gate pulse,voltage across the switch S4 is made zero.Thus zero voltage switching turn on is possible.

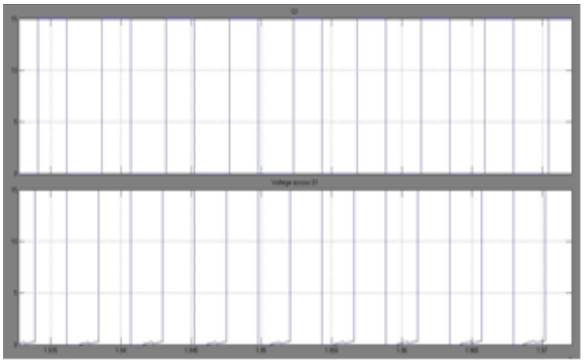

Fig.16. Zero voltage switching in closed loop circuit

Figure15 shows ZVS achieves in closed loop.

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