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A Novel Voltage Gain Multiplier Boost Converter Topology with Ripple Current Cancellation Based on Interleaving Technique

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***Abstract*—The output voltage obtained from renewable energy sources such as PV cells or fuel cells will be usually at low level. This must be boosted up for practical utilization or grid connection. The proposed interleaved boost converter is based on the concept of ripple current cancellation and voltage multiplier extension. This system has the novel feature of reducing the input current ripple. The converter is controlled by interleaved switching pulses, which have the same switching frequency but shifted in phase. Also a multiplier circuit is incorporated in the converter, which enhances the gain. This also helps to reduce the size of input inductor and its corresponding series resistance. These features make the converter ideal to process power from low voltage renewable energy sources. This paper also provides detailed operation and mathematical model of the converter. The results of converter evaluation in MATLAB/Simulink are also included.**

Keywords—Current Ripple Reduction, High Voltage Gain, Interleaved Converter, Multiplier Circuit

I. INTRODUCTION

Dc-Dc converters, converters are greatly used in present industrial electronic devices to obtain desired levels of dc voltage from a dc source. This converters maintain minimal power loss during conversion. Many converter topologies are available such as Boost, Buck, Push pull, Fly back etc. This wide range of selection of converters make it widely accepted amidst current electronic devices.

Green energy sources such Fuel Cells (FC) are finding great acceptance among substitute energy researchers. A FC is a device that converts chemical energy from fuel into electrical energy through chemical reaction with the help of oxygen or oxidizing agents. Due to its high efficiency, low energy consumption and environment friendly nature, FC technology is in progress to commercialize. Higher energy storage capability of FC favors its wide use in automobiles. However suitable power electronic converters are required for enhancing efficient utilization of renewable energy sources. The proposed interleaved multiplier converter is one option for this application.

However in order to link a fuel cell to a load or an inverter, boost converter with large voltage gain at output and lower ripple current at input is required. The major challenge is in designing a converter achieving these features.

II. LITERATURE SURVEY

The basic boost converter is a low cost converter with simple topology and can achieve high voltage gain. But the ideal gain is limited due to inductor series resistance, parasitic losses etc. Therefore basic step up converter is not used when output voltage requirement is higher than four times the input voltage [1]. Further cascaded boost converters came into existence to meet the high voltage requirement [2], [3], [4], [5]. But cascading of converters resulted in increased cost and complexity of control circuit. Further they also suffered from problems associated with high ripple current which resulted in poor efficiency of the converter.

For achieving high voltage gain isolated topologies came into existence that use transformers, [6], [7].Since in this converters voltage gain is proportional to turns ratio, to obtain large voltage gain high turns ratio is required [8]. However large turn's ratio results in high leakage at secondary which in turn increases the switching losses. They also suffer from following disadvantages such as increased transformer loss, increased voltage stress across the device and also results in bulkier circuits.

For improving system efficiency converters without transformers but are still suited for grid connection were necessary .As a solution to this coupled inductors were used to achieve the high voltage gain requirement [9], [10]. Drawbacks of these topologies are, the component count and complex magnetic elements gets increased considerably .Due to these limitations this converter is not used widely. However in all these converters the input ripple current was of least consideration.

Multiphase converters [11] utilize several switching stages. These converters have the advantage of smaller ripple current. But the disadvantage is that duty cycle for zero input ripple current depends on the number of switching stages. Thus the boost factor is limited.

J.C Rosas Caro *et al.*proposed a transformer less boost topology [12] based on duty cycle selection. In this converter both ripple reduction and voltage gain was achieved. However the drawback is that the converter can be designed only for a particular value of duty cycle. And even with switched

capacitance circuit the voltage obtained across each capacitor is not the same.

The interleaved multiplier converter proposed combines the following principles:-

- At the converter's input two inductors are interleaved for cancelling the input current ripple.
- The converter switches is controlled by interleaved switching signals, which have the same switching frequency but shifted in phase.
- At the converter's output switched capacitance voltage multiplier is utilized to increase the voltage gain.
- Voltage multiplier extension circuit is incorporated at the output to further increase the voltage gain and to reduce the size of input inductors.

The paper is organized as follows, Section III provides the details of the proposed converter. Section IV gives the detailed analysis of the converter design. The simulation results are given under Section V. Last but not the least Section VI gives conclusion of this report.

III. PROPOSED CONVERTER TOPOLOGY

The proposed interleaving multiplier converter topology is shown in figure 1.The topology consist of two switches (S_1 and S_2), two energy storing inductors(L_1 *and* L_2),a smaller inductor (L_3), five diodes($d_1 - d_5$), and five capacitors (C_1-C_5). L_3 is used to limit the current through d_3. L_3 is usually around 100 times smaller than L_2 and 50 times smaller than L_1. However selection of L_3 is based on complete charge interchange between C_2 and C_3.

The transistors switch in an interleaved manner with a phase shift of 180 degree [13]. The operation of the converter is elaborated by considering small ripple approximation for voltage across capacitors and continuous conduction mode for L_1 *and* L_2. The proposed topology can be analyzed in three parts, that is, the positive part, negative part and when both switches of the converter are on. The positive part of converter consist of S_1, L_1, C_1, C_4, C_5, d_1, d_4, and d_5.The negative part of the converter consist of S_2, L_2, L_3, C_2, C_3, $d_2$and d_3.

A. Positive Side Switching State Analysis

The converter equivalent circuits resulting from ON and OFF, of switch S_1 are as shown in sections.

- Mode 1

When switch S_1 is closed, the inductor L_1 is connected to the input voltage and current through it raises with a slope equal to v_{in}/L_1 as shown in figure 2 (a).Also when the switch is closed the negative terminals of the capacitors C_1 and C_4 are connected together, allowing C_1 to charge C_4 through d_4 as shown in figure 2 (b).

- Mode 2

When the switch S_1 is open, the inductance current closes d_1 as in traditional boost converter and the inductor current decreases with a slope equal to $(v_{in} - C_1)/L_1$ as shown in figure 2 (a). Also during this time C_5 is charged by C_4 through d_5 as shown in figure 3.

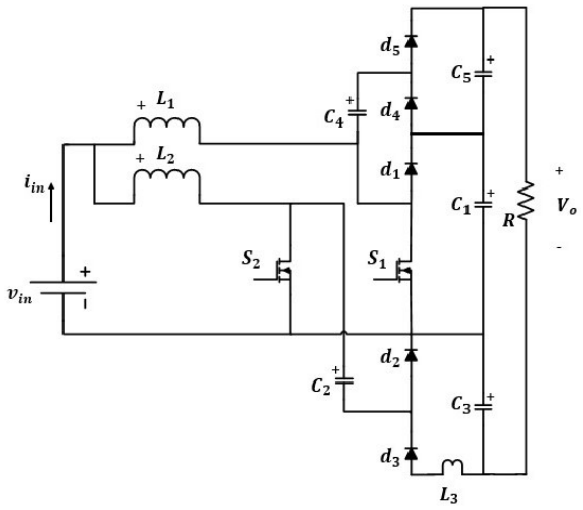

Fig. 1. Circuit schematic of proposed topology

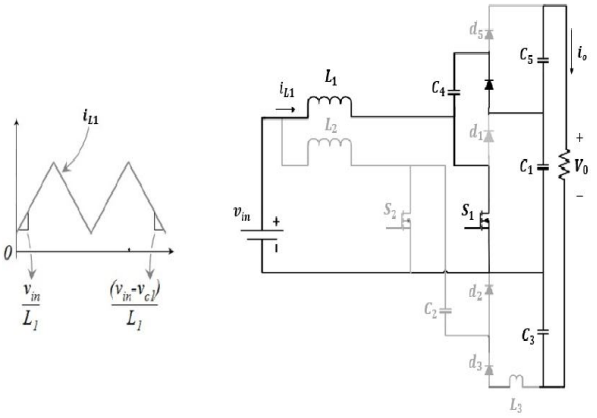

Fig. 2. (a) Waveform of current through inductor L_1 (b) Equivalent circuit schematic when S_1 is ON

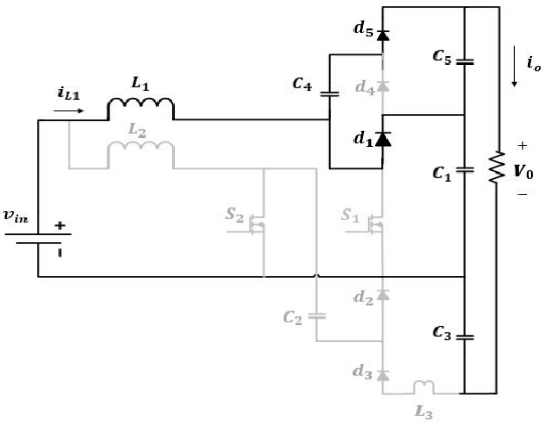

Fig. 3. Equivalent circuit schematic when S_1 is OFF

B. Negative Side Switching State Analysis

The converter equivalent circuits resulting from ON and OFF, of switch S_2 are as shown in section.

- Mode 1

When switch S_2 is closed, the inductor L_2 is connected to the input voltage and current through it raises with a slope equal to v_{in}/L_2 as shown in figure 4 (a).Also when the switch is closed the positive terminals of the capacitors C_2 and C_3 are connected together, allowing C_2 to charge C_3 through d_3 as shown in figure 4 (b).

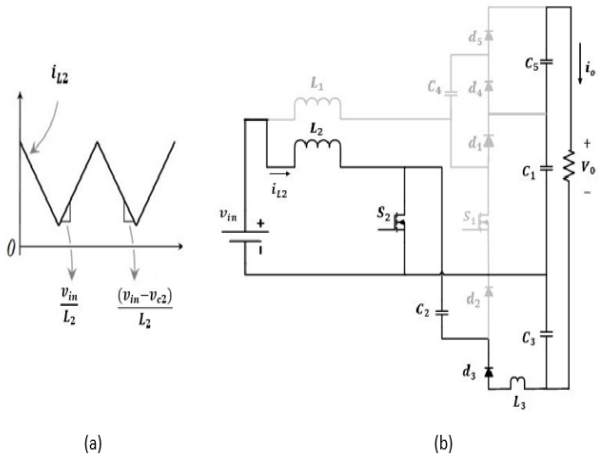

Fig. 4. (a) Waveform of current through inductor L_2 (b) Equivalent circuit schematic when S_2 is ON

- Mode 2

When the switch S_2 is open, the inductance current closes d_2 charging C_2 as shown in figure 5. Also the inductor current decreases with a slope equal to $(v_{in} - C_2)/L_2$ as shown in figure 4 (a).

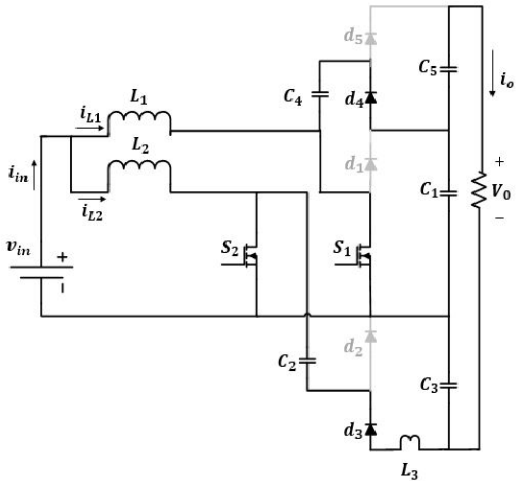

Fig. 5. Equivalent circuit schematic when S_2 is OFF

C. When Both Switches are ON

When both S_1 and S_2 are on, the inductors L_1 and L_2 gets connected to the input voltage and current through the inductors raises with a slope as mentioned in above switching actions.Also when S_1 is closed, the negative terminals of the capacitors C_1 and C_4 are connected together allowing C_1 to charge C_4 through d_4.

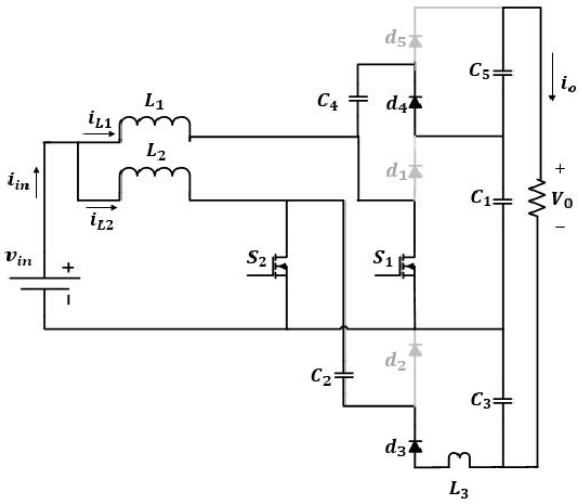

Fig. 6. Equivalent circuit when S_1 ans S_2 are ON

Similarly when S_2 is closed, the positive side of capacitors C_2 and C_3 are connected together allowing C_2 to charge C_3 through d_3 as shown in figure 6.

IV. DESIGN AND ANALYSIS

This section describes the mathematical modelling of the proposed converter. As in figure 1 the proposed architecture corresponds to an interleaving type converter with a phase shift combining features from boost converter, three switch high voltage converter and dc-dc multiplier converter.

A. Voltage Gain

As the state variables feature triangular waveforms similar to those in traditional dc/dc converters the dynamics of L_1, L_2, and C_1 may be conveniently analyzed considering their average behavior. On the other hand,C_2, C_3, and L_3 form a switched capacitance circuit [14], and therefore, their dynamic behavior has to be formulated with additional considerations.

In the circuit with reference to positive side analysis and by using the small ripple approximation the average voltage in the inductorL_1 can be expressed as:

$$L_1 \frac{di_{L1}}{dt} = D_1(v_{in}) + (1 - D_1)(v_{in} - v_{c1}) \quad (1)$$

Where D_1 is the duty cycle of switch S_1, defined as the time the switch keeps closed over the totalswitching period. In steady state, this voltage should be equal zero and then:

$$V_{C1} = \frac{1}{1-D_1} V_{in} \quad (2)$$

Which is the boost factor in the traditional boost converter, during the time when the switch S_1 isclosed, C_4 is charged by C_1 through$d_4$and it gets the same voltage as shown in figure 2 (b).Duringthe time when the switch S_1 is open, C_5 is charged by C_4 through $d_5$and it gets the same voltages shown in Figure 4, and voltage in capacitors C_1 , $C_4$and C_5 can be expressed as:

$$V_{C1} = V_{C4} = V_{C5} = \frac{1}{1-D_1} V_{in} \quad (3)$$

With reference to negative side analysis and by using the small ripple approximation the averagevoltage in the inductor L_2 can be expressed as:

$$L_2 \frac{di_{L2}}{dt} = D_2(v_{in}) + (1 - D_2)(v_{in} - v_{c2}) \quad (4)$$

Where $D_2$is the duty cycle of switch S_2 defined as the time the switch keeps closed over the totalswitching period. In steady state, this voltage should be equal zero and then:

$$V_{C2} = \frac{1}{1-D_2} V_{in} \quad (5)$$

Which is also the boost factor in the traditional boost converter. As shown in figure 5 duringthe time when the switch S_2 is closed, C_3 is charged by C_2 through d_3 , L_3andS_2, and it gets thesame voltage. Therefore the voltage in capacitors C_2 and C_3 can be expressed as:

$$V_{C2} = V_{C3} = \frac{1}{1-D_2} V_{in} \quad (6)$$

Since the output is connected to capacitors C_1 , $C_3$and C_5 and assuming both switches havethe same duty cycle D=D_1=D_2 (because of the interleaving operation) the voltage gain can be
expressed as:

$$\frac{V_o}{V_{in}} = \frac{3}{1-D} \quad (7)$$

The steady-state current through L1 and L2 can be computed by input/output power balance equations. It becomes

$$I_{L1} = I_{L2} = \frac{3}{2} \left(\frac{V_{C1}+V_{C3}+V_{C5}}{R}\right)\left(\frac{1}{1-D}\right) \quad (8)$$

For this proposed converter the operating range is selected to be at D > 0.5, which ensures that L_3 will have enough time to discharge.

B. Energy Storage Inductor Selection

The current ripple on the inductor is given as

$$\Delta i_{L1} = \frac{V_{in}}{L_1} \frac{D}{F_S} \quad (9)$$

$$\Delta i_{L2} = \frac{V_{in}}{L_2} \frac{D}{F_S} \quad (10)$$

where $F_S = \frac{1}{T_S}$is the converters switching frequency. The input current ripple, denoted by Δi_{in},corresponds to the difference between each inductor current ripples, that is,

$$\Delta i_{in} = \frac{V_{in}}{F_S} D \left(\frac{1}{L_2} - \frac{1}{L_1}\right) \quad (11)$$

As it is evident from (11), the input current ripple can be eliminated by zeroing out the left-hand side of this equation. This leads to the following relationship:

$$L_1 = L_2 \quad (12)$$

It is clear from (12) that there is no dependence of the input current ripple with respect to thevalue of the duty cycle. And therefore as the operating point departs from the selected duty ratiothere is no change on the assumption of ripple-free input current.

C. Peak Current Limiting Inductor Selection

As mentioned earlier, the diode d_3 connects the capacitors C_2 and C_3 in parallel, and as a result, a peak- current-limiting inductor is essential. Also, the average current through the diode equals the load current, as it may be evident from figure 7. However, the shape of the current through d_3 may be undesirable and, essential to control it.So to understand thephenomenon, consider the switching process at the time when S_2 turns off. As suggested by figure 8, at that instant, capacitors C_2 and C_3 feature exactly the same voltage because they were connected in parallel. Call this voltage $V_{C.0}$. After S_2 opens, the circuit commutes into the topology in Fig. 1(b), and as a result of this, C_2 and C_3 are no longer connected. While S_2 is off (during $(1 - D)T_S$seconds), C_3 discharges following the load current while C_2 charges following the current through L_2. Call $V_{C3.1}$ and $V_{C3.1}$ the final voltages across capacitors C_2 and C_3, respectively. They can be expressed as

$$V_{C3.1} = V_{C.0} + \Delta v_{C2} = V_{C.0} + \frac{I_{L2}}{C_2}(1 - D)T_S \quad (13)$$

$$V_{C3.1} = V_{C.0} - \Delta v_{C3} = V_{C.0} - \frac{I_0}{C_3}(1 - D)T_S \quad (14)$$

At the end of $(1 - D)T_S$, the voltage difference between them is given by

$$V_{diff} = \Delta v_{C2} + \Delta v_{C3} = \left(\frac{I_{L2}}{C_2} + \frac{I_0}{C_3}\right)(1 - D)T_S \quad (15)$$

If there is no inductor in series with d_3, the peak current would be V_{diff} (some volts) over the resistance in this loop, given by the on-state resistance of S_2 and d_3, and the ESR of C_2 and C_3 (some tens of milliohms). Figure 7 shows a circuit schematic for the current loop where R_{eq} stands for the lumped resistance of the various elements around the loop. This may lead to a peak current that overpasses the peak current limit of the various devices in that loop.

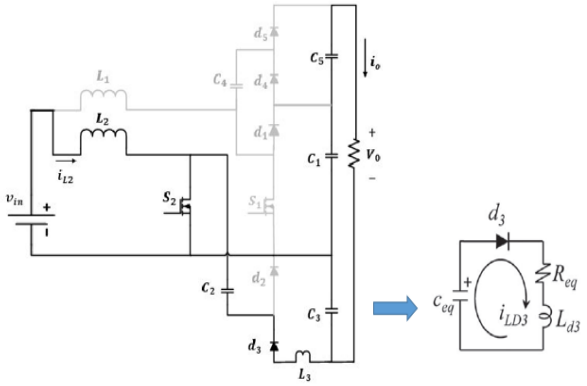

Fig. 7. Equivalent circuit schematics

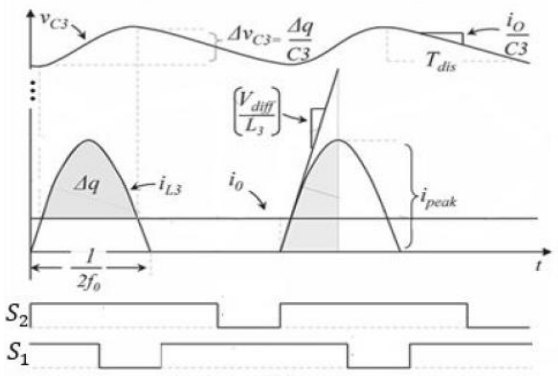

Fig. 8. Waveforms for inductor and capacitor selection

As shown in Figure 8, this current rises rapidly and may destroy power semiconductors if the inductor L_3 is not properly designed. From Figure 7, it is also evident that $C_{eqv.}$ is the series connection of C_2 and C_3. Since L_3 stores a small amount of energy, it charges and discharges completely in a switching period, smoothing out the current through capacitors. It also gives a resonant current peak at a frequency of

$$f_0 = \frac{\omega_0}{2\pi} = \frac{1}{2\pi\sqrt{L_3 C_{eqv.}}} \quad (16)$$

As mentioned above, the converter will operate at a duty cycle larger than 50%. Therefore, L_3 should be selected suchthat $f_0 > F_S$. This ensures that the inductor will complete the discharge process before the beginning of the next switching stage for all values of the duty cycle within the operating range. Furthermore, figure 3.3 provides the basis for calculating the peak current in the loop. At the initial stage of the charging period, the current starts rising at a rate of V_{diff}/L_3 . Hence, representing the current through the loop as $i_{L3}(t) = i_{L3}\sin(\omega_o t)$, its derivative at $t = 0$ can be computed and equated to V_{diff}/L_3. This allows solving for i_{L3}

$$i_{L3} = \frac{V_{diff}}{\omega_o L_3}. \quad (17)$$

D. Capacitor Selection

The selection of the capacitance for C_1, C_2, C_3, $C_4$and C_5 may be approached following a procedure analogous to that used in the sizing of the inductors L_1 and L_2. While S_1 is on, the current through C_1 follows the current through load, and thus

$$\Delta v_{c1} = \frac{I_0}{C_1}(1 - D)T_S \quad (18)$$

Also, while S_1 is closed, the capacitor C_2 charges following the current through L_2, and hence

$$\Delta v_{c2} = \frac{I_{L2}}{C_2}(1 - D)T_S \quad (19)$$

Then C_3 may be selected recognizing that L_3 carries the similar average current as the load. When the value of current at any instant through this inductor crosses the output current, the capacitor C_3 begins its charging, which leads to a voltage increase ΔV_{C3} given by $\Delta q/C_3$. This is graphically shown in figure 8, where the shaded area represents the charge Δq. After L_3 has been selected, the time while C_3 is charging can be computed by finding the time at which $i_0 < i_{L3}(t)$,as suggested in figure 8. Next, C_3 discharges through the remaining of the switching period, and hence

$$T_{dis} = T_S - \left(\frac{2}{\omega_0}\sin^{-1}\left(\frac{i_0}{i_{L3}}\right)\right) \quad (20)$$

where T_{dis} corresponds to the time while C_3 discharges. Since, during this period, C_3 follows the load current, it is possible to state that

$$\Delta v_{c3} = \frac{I_0}{C_3}T_{dis} \quad (21)$$

which allows for the sizing of C_3.While $S_1$is closed C_4gets charged following the current through C_1,i.e the output current I_0 flows through C_4. And also the same I_0flows through C_5 charging it.

$$\Delta v_{c4} = \Delta v_{c5} = \frac{I_0}{C_1}(1 - D)T_{dis} \quad (22)$$

which gives the selection of C_4 and C_5.

V. SIMULINK MODEL AND SIMULATION RESULTS

In this thesis work, for evaluating the performance of the proposed converter topologies and modulations strategies a detailed simulation model has been developed using MATLAB/Simulink software package. The Simulink modelof the converter is designed for an input voltage of V_{in} = 15 V and output voltage of V_o =100 V.The Simulink model of the proposed interleaved multiplier boost converter is shown in Figure 9.The parameter specifications are given in Table 1.

TABLE I. PARAMETER SPECIFICATIONS

Parameters	Values
Duty cycle (D)	55 %
L_1 , L_2 ,L_3	253 μH ,253 μH ,2 μH
C_1 ,C_2 ,C_3	32 μF
R	100
F_S	25 kHz

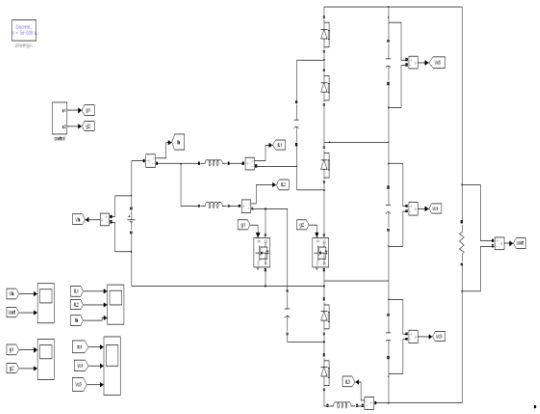

Fig. 9. Simulink model of proposed converter

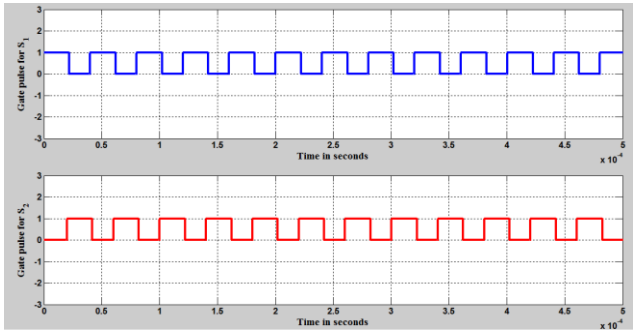

Fig. 10. Gate Pulses for Switches $S_1$and S_2

Figure 10 shows the phase shited gate pulses that is being fed to the switchesS_1 and S_2. Each pulse has a duty ratio of 0.55.The gate pulse fed to S_2 is 180 degree shifted in phase with respect to gate pulse that feeds switch S_1.

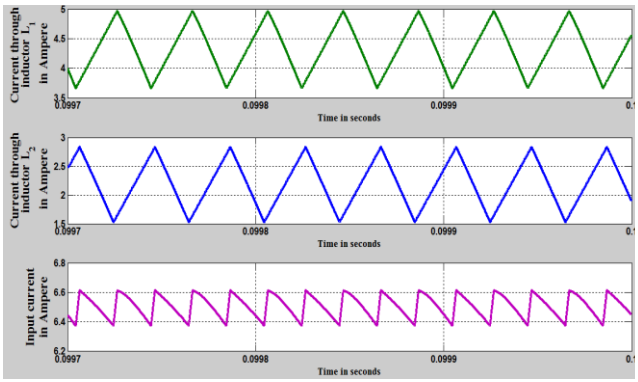

Fig. 11. Waveforms of current through inductors and input current (from result ripple = 0.2)

Figure 11 shows the current through inductors, while the current through L_1 raises the current through L_2falls which results in cancelling of the ripple since input current is the sum of current through $L_1$and L_2.It can be seen that the ripple current is only 0.2 A. Thus the ripple reduction is achieved.

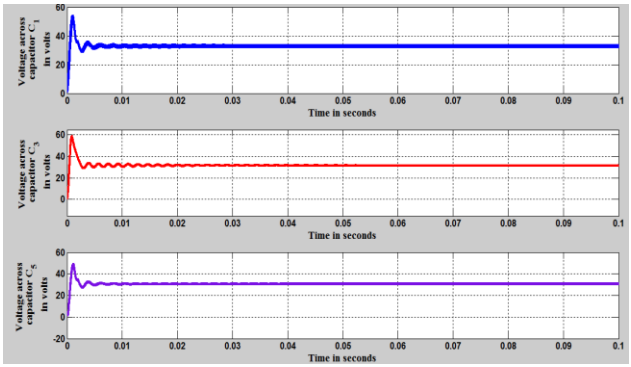

Fig. 12. Waveforms of voltage across C_1, C_3 *and* C_5

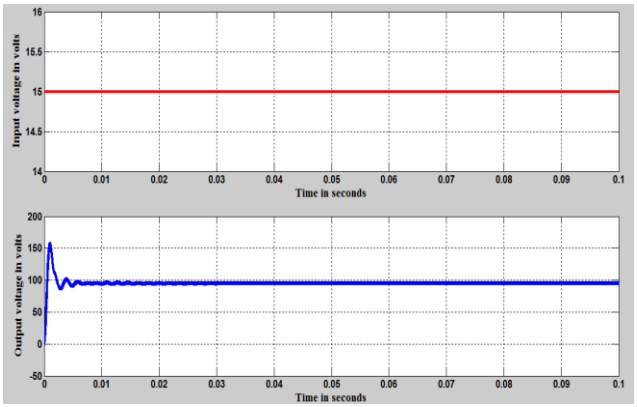

Fig. 13. Waveforms of Input Voltage and Output Voltage

Figure 12 shows the voltage across each capacitor C_1 , C_2 *and* C_3 .It can be seen that voltage across each capacitors are equal and is almost equal to 33 V.Output voltage is the sum of voltage across these capacitors and equal to 100 V as shown in Figure 13.The input voltage supplied is 15 V.

VI. CONCLUSION AND FUTURE SCOPE

The examination of measurements suggest that experimental data are consistent with the analytical results obtained. From the simulation results it is clear that the input current is almost ripple free. Also gain obtained is three times that of conventional boost converter.These features are highly favourable for Fuel cell applications. The proposed converter achieves high voltage gain without extreme duty cycle/boosting transformers. This allows high switching frequency, low voltage stress in switches, modular architecture and more output levels can be added without modifying the basic circuit.

As this converter provides multiple output from the series connected capacitors it can be further modified as to feed a diode clamped multilevel inverter.

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